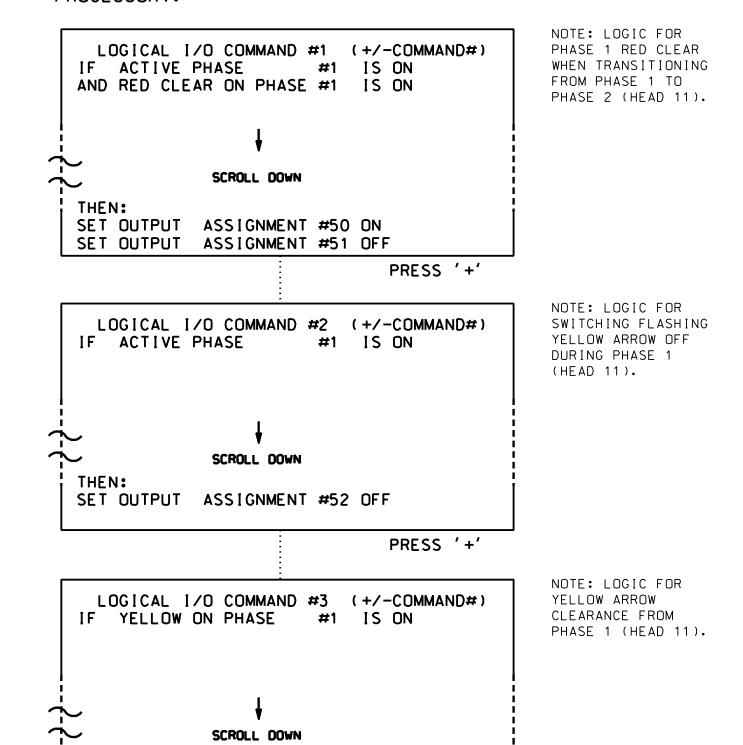
## PROJECT REFERENCE NO. SHEET NO. I - 5714 / U - 5114 Sig. 4.2

## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS). THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

SET OUTPUT ASSIGNMENT #51 ON

THEN:

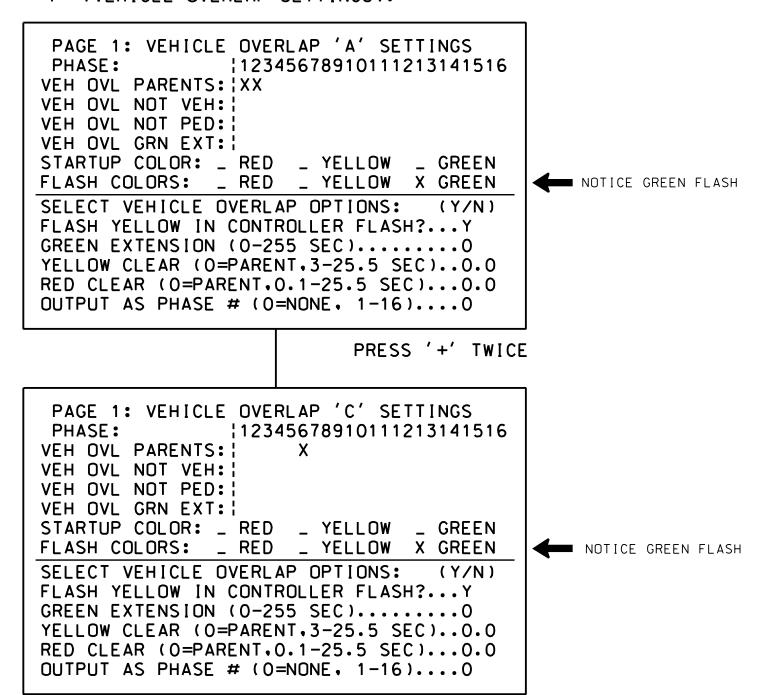
## **OUTPUT REFERENCE SCHEDULE**

OUTPUT 50 = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green

## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN
'1' (VEHICLE OVERLAP SETTINGS).

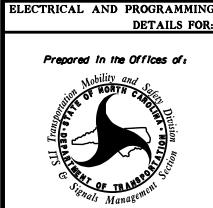


OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 10-1752
DESIGNED: December 2017
SEALED: 04-23-2018
REVISED: N/A

Electrical Detail - Sheet 2 of 2

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



SR 2136 (Gilead Road)
at
SR 2138 (McCov Boad)

SR 2138 (McCoy Road)
Division 10 Mecklenburg Co. Hunte

PLAN DATE: December 2017 REVIEWED BY: A.D. Klinksiek
PREPARED BY: J.T. Thibault REVIEWED BY: N.R. Simmons
REVISIONS INIT. DATE

SEAL 031464

OCCUSIGNED BY

ACTION AT URE

OCCUSION AT UR

**SIG.** INVENTORY NO. 10-1752

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