PROJECT REFERENCE NO.	SHEET NO.
U-4405	SIG-37.3

ECONOLITE ASC/3-2070 LOGIC PROCESSOR PROGRAMMING DETAIL

(program controller as shown)

1. From Main Menu select | 1. CONFIGURATION |

2. From CONFIGURATION Submenu select | 8. LOGIC PROCESSOR |

3. From LOGIC PROCESSOR Submenu select | 2. LOGIC STATEMENTS |

ENTER A "1" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   1  COPY FROM:   1  ACTIVE:  M   FALSE
IF    CTR PHASE TMING      1      IS ON
THEN  SIG SET OLP GREEN    1         OFF

ELSE
```
LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING PHASE 1 (HEADS 83,84)

ENTER A "2" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   2  COPY FROM:   2  ACTIVE:  M   FALSE
IF    VEH YELLOW ON PH     1      IS ON
THEN  SIG SET OLP YELLOW   1         ON

ELSE
```
LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83,84)

ENTER A "3" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   3  COPY FROM:   3  ACTIVE:  M   FALSE
IF    VEH RED ON PHASE     1      IS ON
AND   CTR PHASE TIMING     1      IS ON
THEN  SIG SET OLP RED      1         ON

ELSE
```
LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 1 (HEADS 83,84)

ENTER A "4" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   4  COPY FROM:   4  ACTIVE:  M   FALSE
IF    VEH OVERLAP          7      IS ON
THEN  SIG SET OVLP GREEN   2         OFF

ELSE
```
LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING OLG, WHICH HAS PARENT PHASE 7 (HEAD 63)

ENTER A "5" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   5  COPY FROM:   5  ACTIVE:  M   FALSE
IF    VEH OVERLAP YLW      7      IS ON
THEN  SIG SET OLP YELLOW   2         ON

ELSE
```
LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING OLG, WHICH HAS PARENT PHASE 7 (HEAD 63)

ENTER A "6" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   6  COPY FROM:   6  ACTIVE:  M   FALSE
IF    VEH OVERLAP          7      IS ON
AND   VEH OVERLAP RED      7      IS ON
THEN  SIG SET OLP RED      2         ON

ELSE
```
LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING OLG, WHICH HAS PARENT PHASE 7 (HEAD 63)

ENTER A "7" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   7  COPY FROM:   7  ACTIVE:  M   FALSE
IF    CTR PHASE TMING      5      IS ON
THEN  SIG SET OLP GREEN    3         OFF

ELSE
```
LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING PHASE 5 (HEAD 43)

ENTER A "8" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   8  COPY FROM:   8  ACTIVE:  M   FALSE
IF    VEH YELLOW ON PH     5      IS ON
THEN  SIG SET OLP YELLOW   3         ON

ELSE
```
LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING PHASE 5 (HEAD 43)

ENTER A "9" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:   9  COPY FROM:   9  ACTIVE:  M   FALSE
IF    VEH RED ON PHASE     5      IS ON
AND   CTR PHASE TIMING     5      IS ON
THEN  SIG SET OLP RED      3         ON

ELSE
```
LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING PHASE 5 (HEAD 43)

ENTER A "10" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:  10  COPY FROM:  10  ACTIVE:  M   FALSE
IF    VEH OVERLAP          8      IS ON
THEN  SIG SET OVLP GREEN   4         OFF

ELSE
```
LOGIC FOR TURNING FLASHING YELLOW ARROW OFF DURING OLH, WHICH HAS PARENT PHASE 3 (HEAD 24)

ENTER A "11" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:  11  COPY FROM:  11  ACTIVE:  M   FALSE
IF    VEH OVERLAP YLW      8      IS ON
THEN  SIG SET OLP YELLOW   4         ON

ELSE
```
LOGIC FOR YELLOW ARROW CLEARANCE WHEN LEAVING OLH, WHICH HAS PARENT PHASE 3 (HEAD 24)

ENTER A "12" IN THE LP# FIELD, PRESS 'ENTER', AND PROGRAM AS SHOWN.

```
LP#:  12  COPY FROM:  12  ACTIVE:  M   FALSE
IF    VEH OVERLAP          8      IS ON
AND   VEH OVERLAP RED      8      IS ON
THEN  SIG SET OLP RED      4         ON

ELSE
```
LOGIC FOR RED SIGNAL CLEARANCE WHEN LEAVING OLH, WHICH HAS PARENT PHASE 3 (HEAD 24)

END PROGRAMMING

---

4. From LOGIC PROCESSOR Submenu select | 1. LOGIC STATEMENT CONTROL |

ENABLE LOGIC PROCESSOR STATEMENTS 1–12 BY POSITIONING THE CURSOR OVER THE FIELDS SHOWN BELOW AND USING THE TOGGLE KEY TO ENABLE THEM.

```
LOGIC STATEMENT CONTROL
          1 2 3 4 5 6 7 8 9 0 1 2 3 4 5
LP 1-15   E E E E E E E E E E E E . . .
LP 16-30  . . . . . . . . . . . . . . .
LP 31-45  . . . . . . . . . . . . . . .
LP 46-60  . . . . . . . . . . . . . . .
LP 61-75  . . . . . . . . . . . . . . .
LP 76-90  . . . . . . . . . . . . . . .
```

END PROGRAMMING

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 06-0155T2
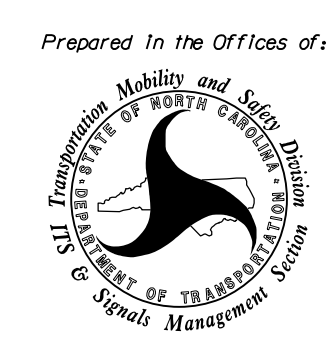DESIGNED: March 2018
SEALED: 03-29-2018
REVISED: N/A

Temporary Design 2 - TMP Phase II
Electrical Detail - Sheet 3 of 3

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

Stantec

Stantec Consulting Services Inc.
801 Jones Franklin Road-Suite 300
Raleigh, NC 27606
Tel. (919) 851-6866
Fax. (919) 851-7024
www.stantec.com
License No. F-0672

ELECTRICAL AND PROGRAMMING DETAILS FOR:
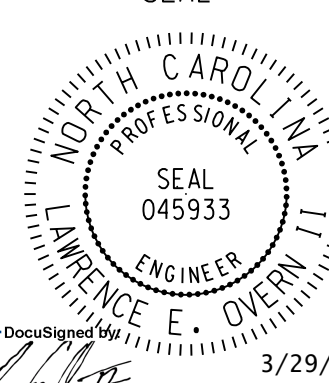
Prepared in the Offices of:

750 N.Greenfield Pkwy,Garner,NC 27529

US 401 Business (Raeford Road) at NC 59 (Hope Mills Road)/ SR 1592 (Glensford Drive)

Division 6	Cumberland County	Fayetteville
PLAN DATE: March 2018	REVIEWED BY: L Overn	
PREPARED BY: G B Spell	REVIEWED BY:	

REVISIONS			
	INIT.	DATE	

SEAL

NORTH CAROLINA
PROFESSIONAL
SEAL
045933
LAWRENCE E. OVERN II
ENGINEER

3/29/2018

SIG. INVENTORY NO. 06-0155T2