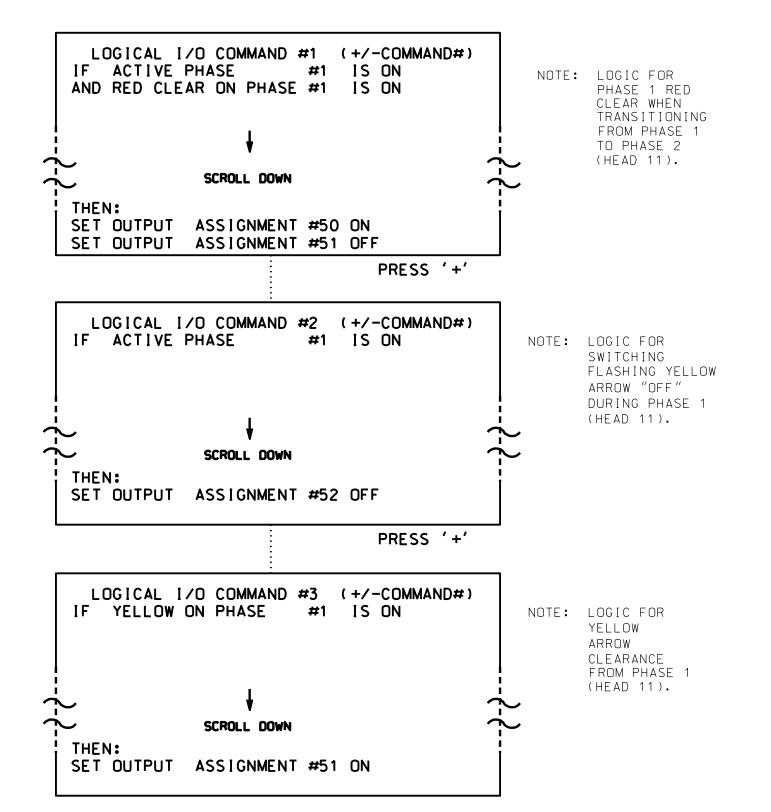
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL

TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL). THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1. 2. AND 3. LOGIC COMMANDS 4. 5. AND 6 ARE TO BE DISABLED IN THIS TEMPORARY PHASE.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS). THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

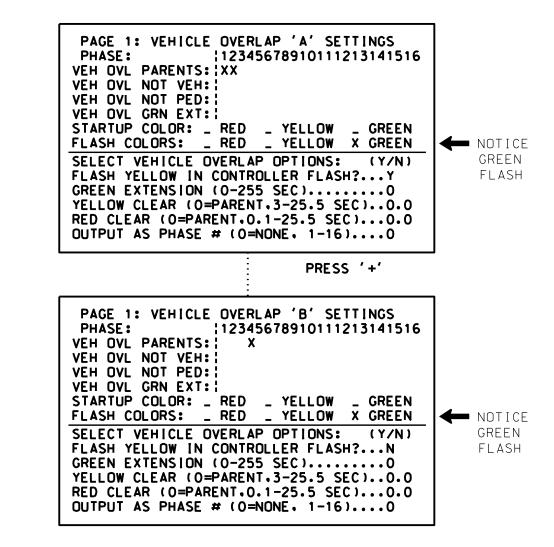
OUTPUT REFERENCE SCHEDULE USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 50 = Overlap A Red OUTPUT 51 = Overlap A Yellow OUTPUT 52 = Overlap A Green U-5169 Sig. 20.2

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS).
THEN '1' (VEHICLE OVERLAP SETTINGS).

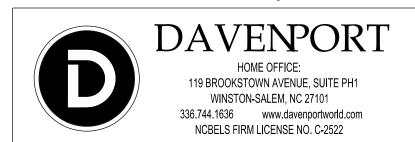


OVERLAP PROGRAMMING COMPLETE

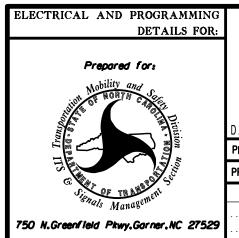
THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1470T4 DESIGNED: May 2018 SEALED: May 20, 2018 REVISED: N/A

Project #: 170908

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



Temporary Design 4; TMP-36,39 Electrical Detail - Sheet 2 of 3



NC 68 (Eastchester Dr.)
at

Cypress Ct.

ivision 7 Guilford County High Po

LAN DATE: May 2018 REVIEWED BY: L. Boyer

PLAN DATE: May 2018 REVIEWED BY: L. Boyer
PREPARED BY: A. Ravipati REVIEWED BY:

REVISIONS INIT. DATE

SEAL

SEAL

SEAL

O32117

Docusigned by:

3. Royal Hinshan 05/20/201

SIGNATURE DATE

SIGNATURE DATE

SIGN INVENTORY NO. 07-1470T4