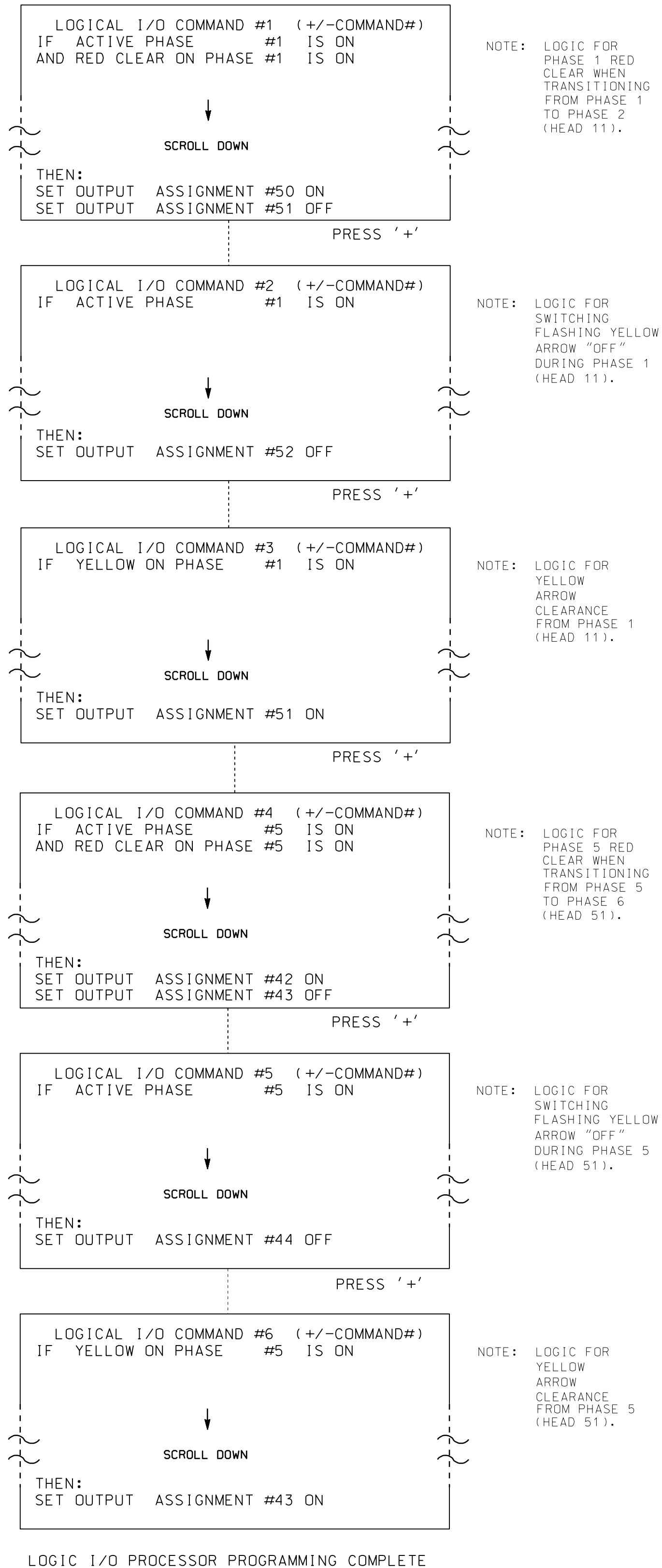


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, AND 6.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

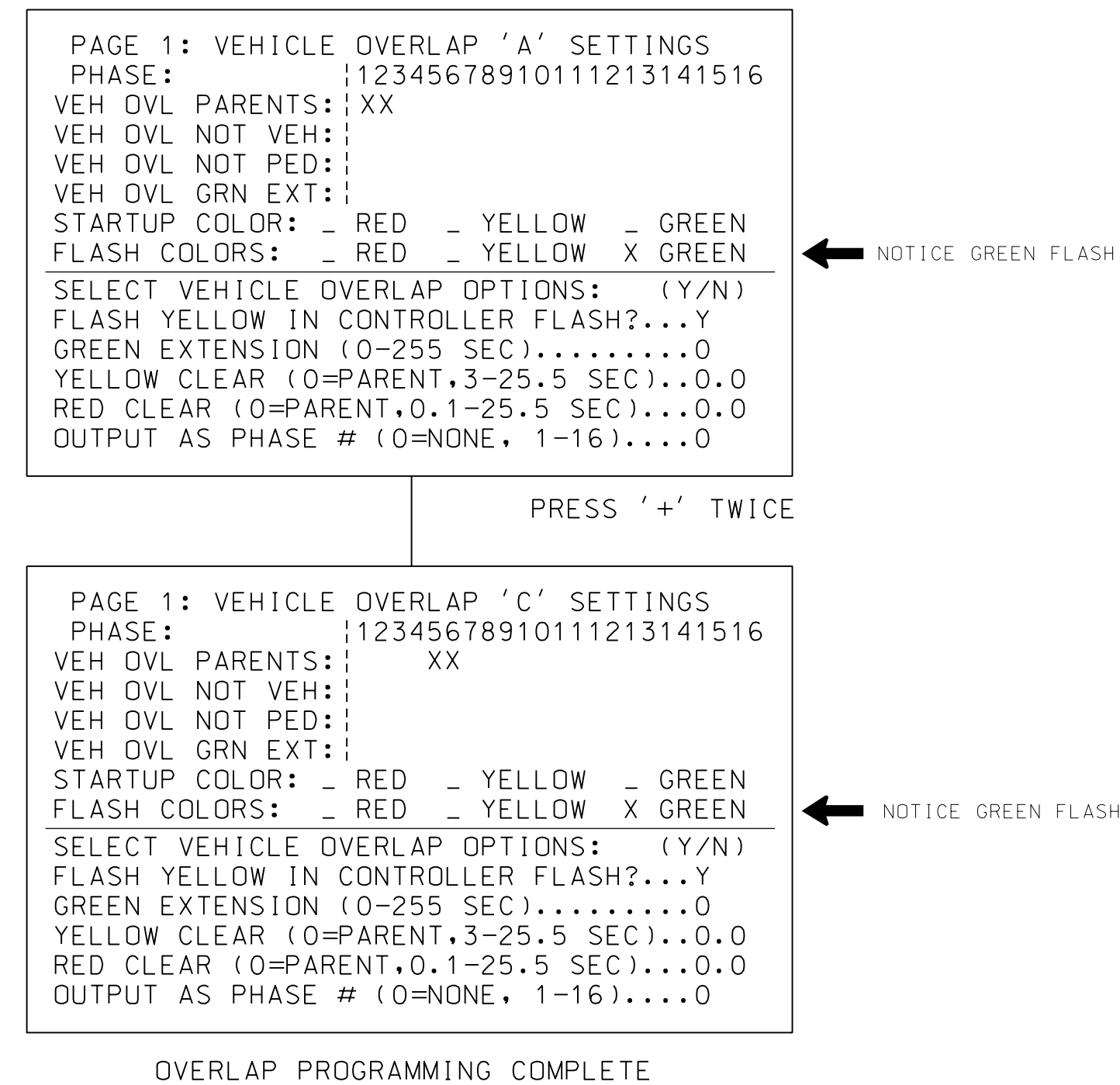


LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow
OUTPUT 44 = Overlap C Green

OUTPUT 50 = Overlap A Red
OUTPUT 51 = Overlap A Yellow
OUTPUT 52 = Overlap A Green

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 12-0981-T1
DESIGNED: July 2016
SEALED: 10/4/2016
REVISED:



Stantec Consulting Services Inc.
801 Jones Franklin Road
Suite 300
Raleigh, NC 27606
Tel. (919) 851-6866
Fax. (919) 851-7024
www.stantec.com
License No. F-0672

Signal Upgrade
Temporary Detail 1 - TMP Phases 1 & 01A
ELECTRICAL DETAIL SHEET 2 OF 2

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

	NC 273 (Highland St/S.Main St) at S.Main St/ Shopping Center Entrance	
	Division 12 PLAN DATE: JULY 2016 PREPARED BY: J. HAMBRIGHT	Mount Holly REVIEWED BY: D. HARRIS REVIEWED BY: B. WATSON
REVISIONS INIT. DATE	SEAL 29449 P. WATSON	Documented by: Betsy L. Watson 10/4/2016 DATE SIG. INVENTORY NO. 12-0981-T1