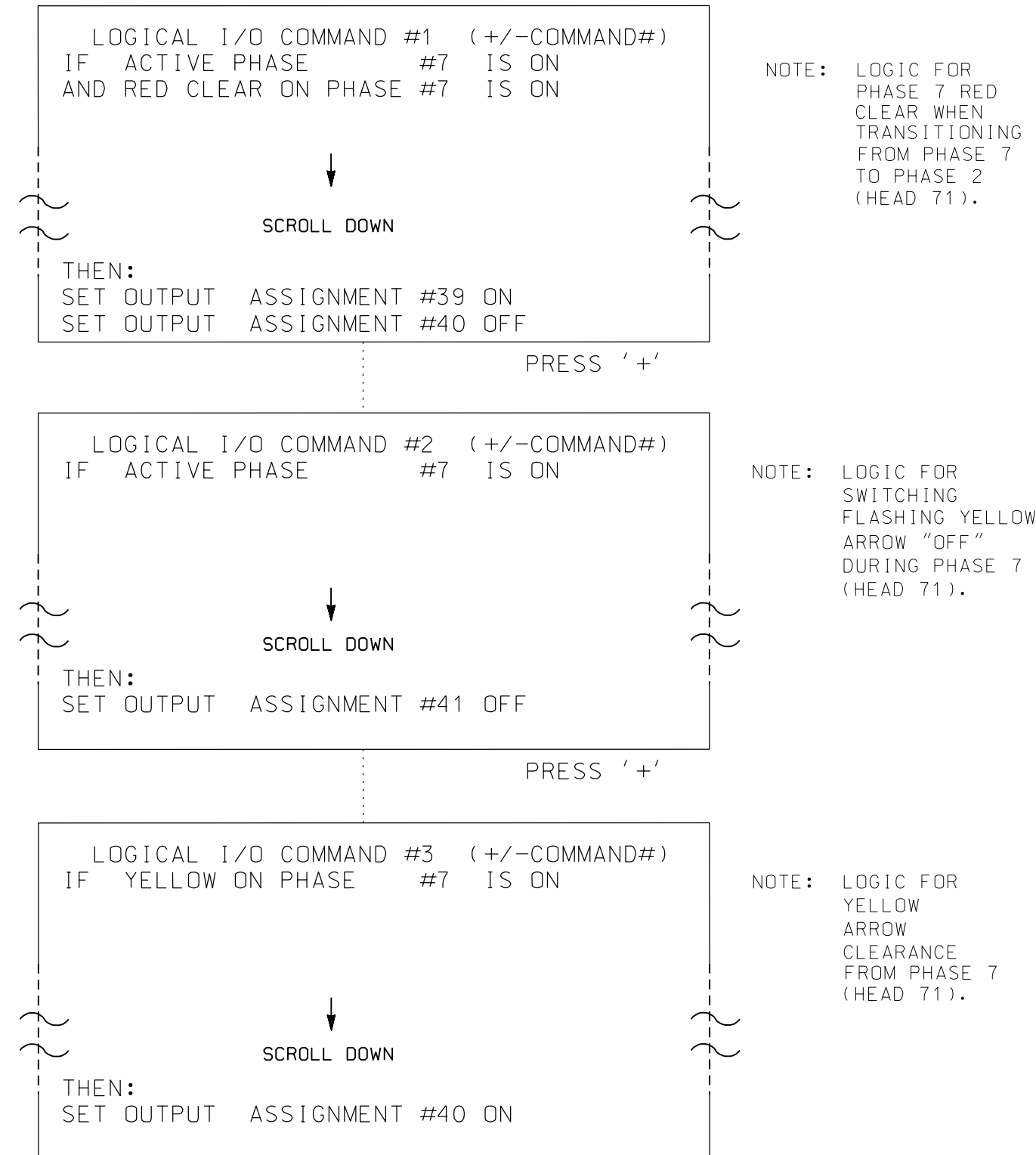


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OUTPUT REFERENCE SCHEDULE	
OUTPUT 39	= Overlap D Red
OUTPUT 40	= Overlap D Yellow
OUTPUT 41	= Overlap D Green

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

- FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

```

    PRESS '+' THREE TIMES
    PAGE 1: VEHICLE OVERLAP 'D' SETTINGS
    PHASE:      |12345678910111213141516
    VEH OVL PARENTS: | X   X
    VEH OVL NOT VEH: |
    VEH OVL NOT PED: |
    VEH OVL GRN EXT: |
    STARTUP COLOR:  | _ RED _ YELLOW _ GREEN
    FLASH COLORS:   | _ RED _ YELLOW X GREEN
    SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
    FLASH YELLOW IN CONTROLLER FLASH?...Y
    GREEN EXTENSION (0-255 SEC)...0
    YELLOW CLEAR (0=PARENT,3-25.5 SEC)...0
    RED CLEAR (0=PARENT,0.1-25.5 SEC)...0
    OUTPUT AS PHASE # (0=NONE, 1-16)...0
  
```

OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)

- FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS NEXT TO ADVANCE TO PAGE 2.

```

    PRESS '+' THREE TIMES
    PAGE 2: VEHICLE OVERLAP 'D' SETTINGS
    PHASE:      |12345678910111213141516
    VEH OVL PARENTS: |           X
    VEH OVL NOT VEH: |
    VEH OVL NOT PED: |
    VEH OVL GRN EXT: |
    STARTUP COLOR:  | _ RED _ YELLOW _ GREEN
    FLASH COLORS:   | _ RED _ YELLOW _ GREEN
    SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
    FLASH YELLOW IN CONTROLLER FLASH?...Y
    GREEN EXTENSION (0-255 SEC)...0
    YELLOW CLEAR (0=PARENT,3-25.5 SEC)...0
    RED CLEAR (0=PARENT,0.1-25.5 SEC)...0
    OUTPUT AS PHASE # (0=NONE, 1-16)...0
  
```

OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR
THE SIGNAL DESIGN: 10-2188
DESIGNED: June 2015
SEALED: August 30, 2015
REVISED:

ELECTRICAL DETAIL SHEET 2 OF 4

**DOCUMENT NOT CONSIDERED FINAL
UNLESS ALL SIGNATURES COMPLETED**

PLANS PREPARED BY:

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ELECTRICAL AND PROGRAMMING
DETAILS FOR:

Prepared for the Offices of:

750 N. Greenfield Pkwy, Garner, NC 27529

US 74 (Independence Blvd) EB at SR 1367 (Unionville-Indian Trail Road)	
Division 10	Indian Trail
PLAN DATE: June 2015	REVIEWED BY: LM Moon
PREPARED BY: K Smith	REVIEWED BY: B Humfleet
REVISIONS	INIT. DATE

SEAL

Lisa M. Moon 12/12/2016
DATE

SIG. INVENTORY NO. 10-2188

09-BEC-2016_14-15
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