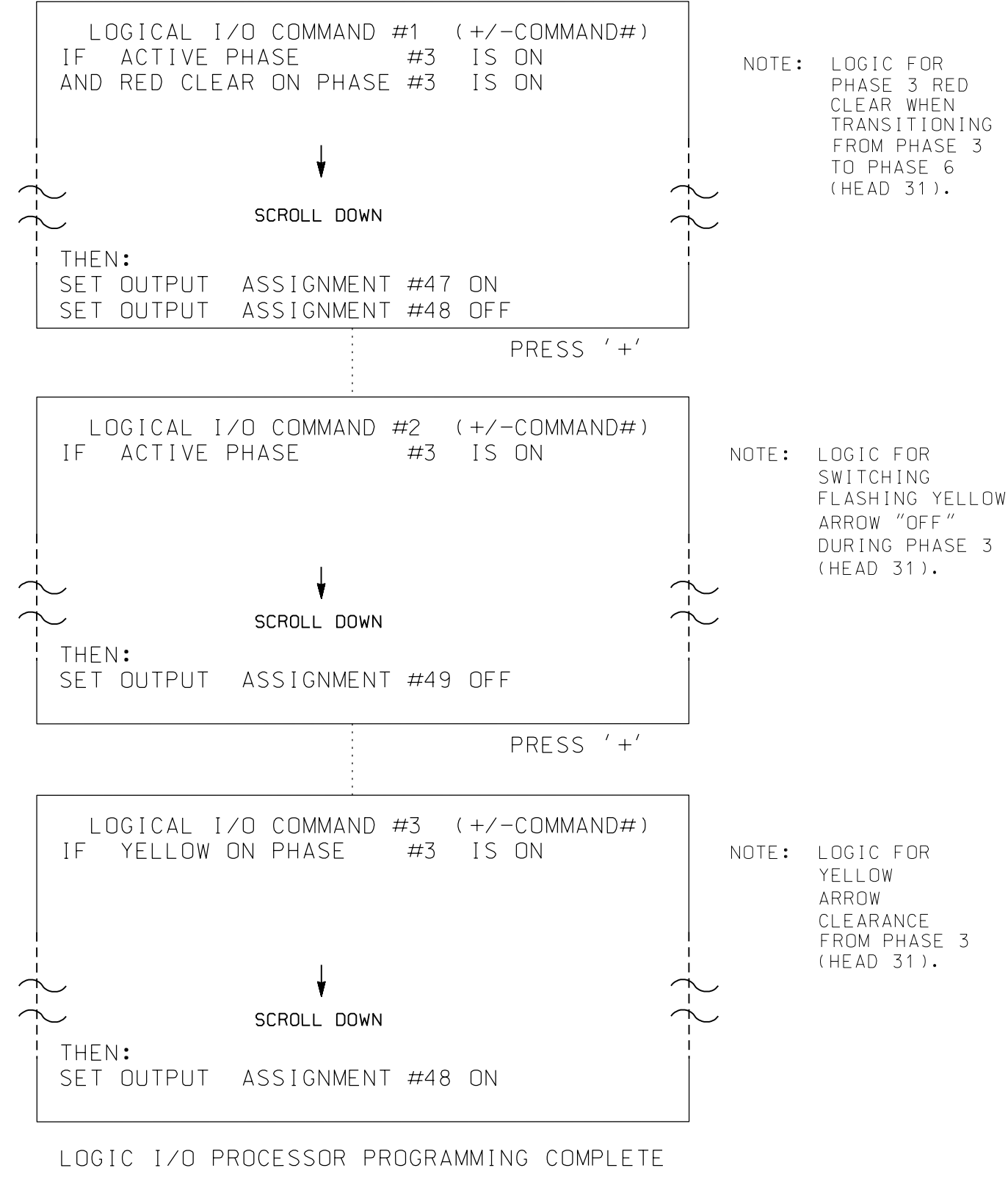


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, and 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT REFERENCE SCHEDULE

USE TO INTERPRET LOGIC PROCESSOR

OUTPUT 47 = Overlap B Red
OUTPUT 48 = Overlap B Yellow
OUTPUT 49 = Overlap B Green

OVERLAP PROGRAMMING DETAIL FOR DEFAULT PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+'

PAGE 1: VEHICLE OVERLAP 'B' SETTINGS
PHASE: |12345678910111213141516
VEH OVL PARENTS: | X X
VEH OVL NOT VEH: |
VEH OVL NOT PED: |
VEH OVL GRN EXT: |
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN ← NOTICE GREEN FLASH
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)...0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0

OVERLAP PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL FOR ALTERNATE PHASING

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS). PRESS NEXT TO ADVANCE TO PAGE 2.

PRESS '+'

NOTICE PAGE 2 →

PAGE 2: VEHICLE OVERLAP 'B' SETTINGS
PHASE: |12345678910111213141516
VEH OVL PARENTS: | X
VEH OVL NOT VEH: |
VEH OVL NOT PED: |
VEH OVL GRN EXT: |
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW - GREEN
SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)...0
YELLOW CLEAR (0=PARENT,3-25.5 SEC)...0.0
RED CLEAR (0=PARENT,0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0

OVERLAP PROGRAMMING COMPLETE

COUNTDOWN PEDESTRIAN SIGNAL OPERATION

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 10-2187
DESIGNED: June 2015
SEALED: November 11, 2016
REVISED:

ELECTRICAL DETAIL SHEET 2 OF 4

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED



Division 10	Union County	Indian Trail
PLAN DATE: June 2015	REVIEWED BY: LW Moon	
PREPARED BY: K Smith	REVIEWED BY: B Humfleet	
REVISIONS	INIT.	DATE

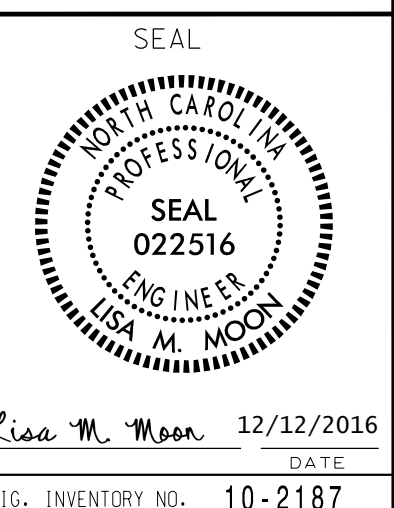
US 74 (Independence Blvd) WB
at
SR 1367 (Unionville-Indian Trail Road)

Division 10 Union County Indian Trail

PLAN DATE: June 2015 REVIEWED BY: LW Moon

PREPARED BY: K Smith REVIEWED BY: B Humfleet

REVISIONS INIT. DATE



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