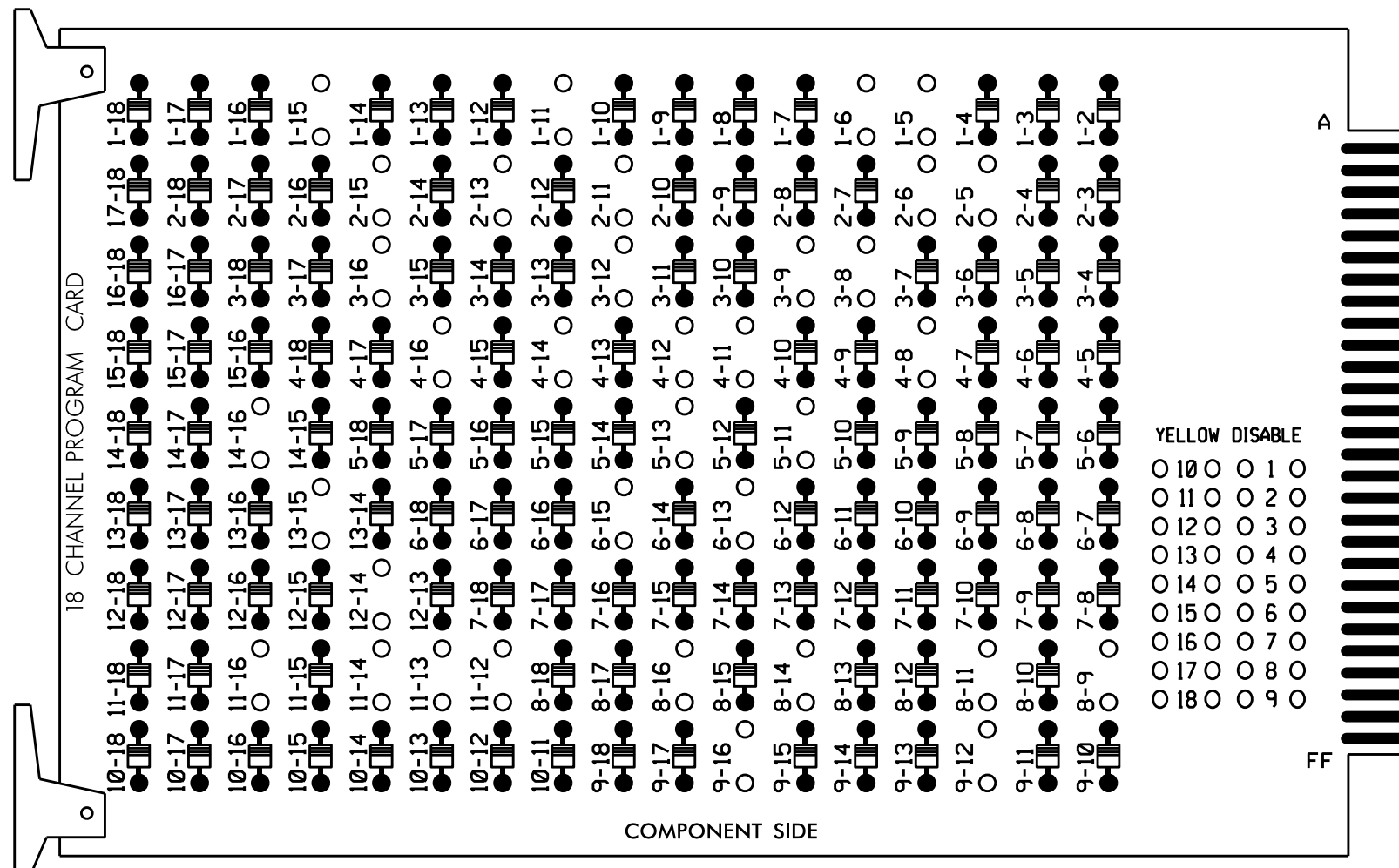


EDI MODEL 2018ECLIP-NC CONFLICT MONITOR PROGRAMMING DETAIL

(remove jumpers and set switches as shown)

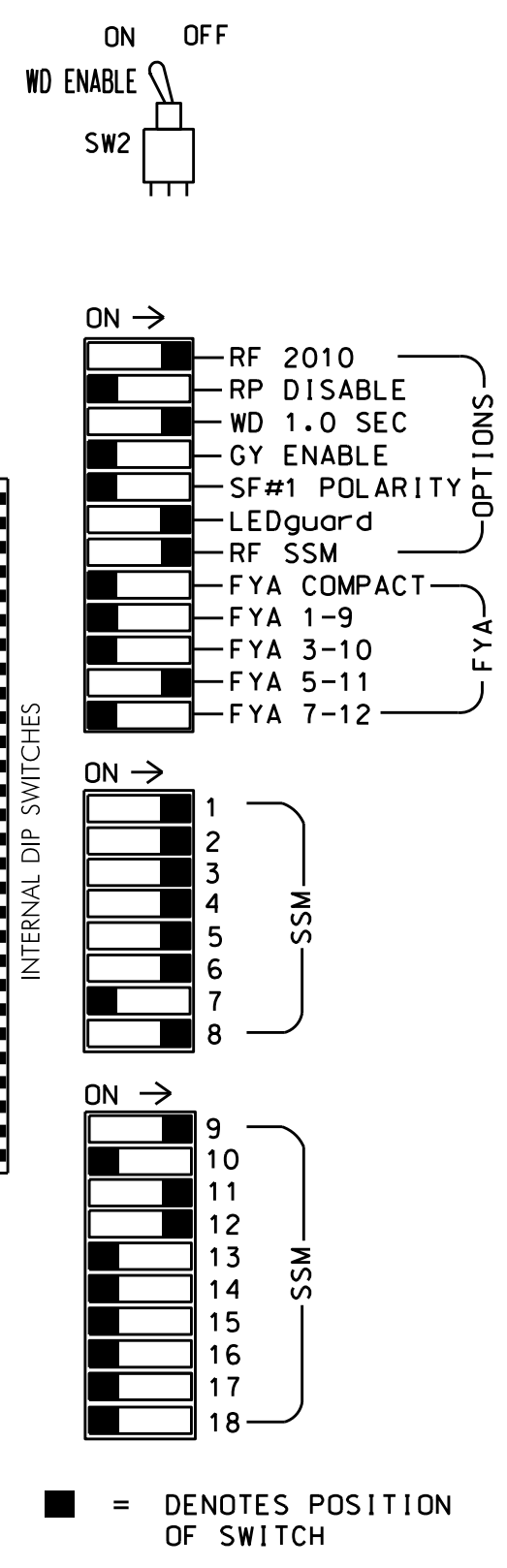
REMOVE DIODE JUMPERS 1-5, 1-6, 1-11, 1-15, 2-5, 2-6, 2-11, 2-13, 2-15, 3-8, 3-9, 3-12, 3-16, 4-8, 4-11, 4-12, 4-14, 4-16, 5-11, 5-13, 6-13, 6-15, 8-9, 8-11, 8-14, 8-16, 9-12, 9-16, 11-2, 11-13, 11-14, 11-16, 12-14, 13-15, and 14-16.



REMOVE JUMPERS AS SHOWN

NOTES:

- Card is provided with all diode jumpers in place. Removal of any jumper allows its channels to run concurrently.
- Ensure jumpers SEL2-SEL5 and SEL9 are present on the monitor board.
- Ensure that Red Enable is active at all times during normal operation.
- Integrate monitor with Ethernet network in cabinet.



- ### NOTES
- To prevent "flash-conflict" problems, insert red flash program blocks for all unused vehicle load switches in the output file. The installer shall verify that signal heads flash in accordance with the Signal Plans.
 - Enable Simultaneous Gap-Out for all phases.
 - Program phases 2 and 6 for volume density operation.
 - Program controller to start up in phase 2 Walk and 6 Walk.
 - The cabinet and controller are part of the Fayetteville Signal System.

EQUIPMENT INFORMATION

CONTROLLER.....2070E
 CABINET.....332 W/ AUX
 SOFTWARE.....ECONOLITE ASC/3-2070
 CABINET MOUNT.....BASE
 OUTPUT FILE POSITIONS...18 WITH AUX. OUTPUT FILE
 LOAD SWITCHES USED.....S1,S2,S3,S4,S5,S6,S7,S8,S9,
 S11,S12,AUX S1,AUX S4,AUX S5
 PHASES USED.....1,2,2PED,3,4,4PED,5,6,6PED,
 7*,8,8PED,9**

OVERLAP A.....3
 OVERLAP B.....NOT USED
 OVERLAP C.....4+5+9
 OVERLAP D.....7+9
 OVERLAP P.....1+2+3+4+5+6+7+8

* Used for timing purposes only.
 ** Used during preempt only.

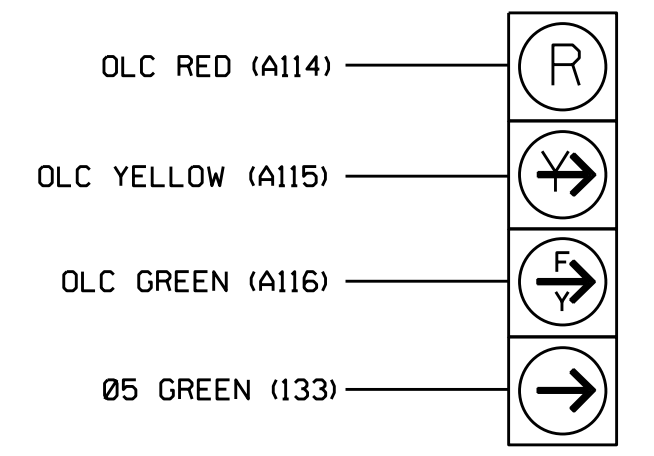
SIGNAL HEAD HOOK-UP CHART

LOAD SWITCH NO.	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	AUX S1	AUX S2	AUX S3	AUX S4	AUX S5	AUX S6						
CMU CHANNEL NO.	1	2	13	3	4	14	5	6	15	7	8	16	9	10	17	11	12	18						
PHASE	1	2	2 PED	3	4	4 PED	5	6	6 PED	7	8	8 PED	OLA	OLB	SPARE	OLC	OLD	SPARE						
SIGNAL HEAD NO.	11,12	82	21,22	P21, P22	31,32	41,42	P41, P42	51,52	53,54	61,62	P61, P62	NC	81,82	P81, P82	22	NU	NU	53,54	62	71,72	NU			
RED			128			101				134			107	*					A114					
YELLOW			129			102				135			108											
GREEN			130			103				136			109											
RED ARROW	125					116				131												A101		
YELLOW ARROW	126	126				117				132						A122						A115	A102	A102
FLASHING YELLOW ARROW																						A116		
GREEN ARROW	127	127				118				133	133					A123							A103	A103
Hand							113			104			119									110		
Walking																								112

NU = Not Used
 NC = Not Connected
 * Denotes install load resistor. See load resistor installation detail this sheet.
 ★ See pictorial of head wiring in detail below.

FYA SIGNAL WIRING DETAIL

(wire signal head as shown)



53,54

NOTE

The sequence display for signal heads 53 and 54 requires special logic programming. See sheet 4 for programming instructions.

COUNTDOWN PEDESTRIAN SIGNAL OPERATION

Countdown Ped Signals are required to display timing only during Ped Clearance Interval. Consult Ped Signal Module user's manual for instructions on selecting this feature.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 06-0527
 DESIGNED: February 2016
 SEALED: 9/9/2016
 REVISED: N/A

Electrical Detail - Sheet 1 of 4

DOCUMENT NOT CONSIDERED FINAL UNLESS ALL SIGNATURES COMPLETED

	SR 1400 (Cliffdale Road) at SR 1596 (Glensford Drive)/ Glensford Drive Extension Division 6 Cumberland County Fayetteville PLAN DATE: September 2016 REVIEWED BY: PREPARED BY: S. Armstrong REVIEWED BY: REVISIONS: _____ INIT. DATE: _____ 750 N. Greenfield Pkwy, Garner, NC 27529	
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Signed by: Keith M. Mims 9/22/2016
 DATE: _____
 SIG. INVENTORY NO. 06-0527

INPUT FILE POSITION LAYOUT

(front view)

FILE	U	1	2	3	4	5	6	7	8	9	10	11	12	13	14
"I"	U	Ø 1	Ø 1	Ø 2	S	S	Ø 3	Ø 4	S	S	S	S	Ø 2 PED	Ø 6 PED	FS
	L	1A	1B	2A	STOP	STOP	3A	4A	STOP	STOP	STOP	STOP	DC ISOLATOR	DC ISOLATOR	DC ISOLATOR
"J"	U	NOT USED	Ø 1	Ø 2	Y	Y	Ø 3	Ø 4	Y	Y	Y	Y	Ø 4 PED	Ø 8 PED	ST
	L	1C	2B	Y	Y	3B	4B	Y	Y	Y	Y	Y	DC ISOLATOR	DC ISOLATOR	DC ISOLATOR
"U"	U	Ø 5	Ø 5	Ø 5	Ø 6	S	Ø 7/9	Ø 8	S	S	S	S	S	S	PRE1
	L	5A	5B	5D	6B	STOP	7A	8A	STOP	STOP	STOP	STOP	STOP	STOP	AC ISOLATOR
"J"	U	NOT USED	Ø 5	Ø 6	NOT USED	Y	Ø 7/9	Ø 8	Y	Y	Y	Y	Y	Y	NOT USED
	L	5C	6A	NOT USED	Y	Y	7B	8B	Y	Y	Y	Y	Y	Y	NOT USED

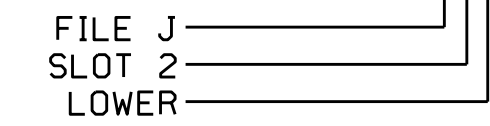
EX.: 1A, 2A, ETC. = LOOP NO.'S
 FS = FLASH SENSE
 ST = STOP TIME
 PRE1 = RR PREEMPT

INPUT FILE CONNECTION & PROGRAMMING CHART

LOOP NO.	LOOP TERMINAL	INPUT FILE POS.	PIN NO.	DETECTOR NO.	NEMA PHASE	CALL	EXTEND TIME	DELAY TIME	DETECTOR TYPE
1A	TB2-1,2	I1U	56	1	1	YES		3	S
1B	TB2-5,6	I2U	39	2	1	YES			S
1C	TB2-7,8	I2L	43	12	1	YES		15	S
2A	TB2-9,10	I3U	63	32	2	YES			N
2B	TB2-11,12	I3L	76	42	2	YES			N
3A	TB4-9,10	I6U	41	4	3	YES			S
3B	TB4-11,12	I6L	45	14	3	YES			S
4A	TB6-1,2	I7U	65	34	4	YES			S
4B	TB6-3,4	I7L	78	44	4	YES			S
5A	TB3-1,2	J1U	55	5	5	YES		3	S
5B	TB3-5,6	J2U	40	6	5	YES			S
5C	TB3-7,8	J2L	44	16	5	YES		15	S
5D	TB3-9,10	J3U	64	36	5	YES		15	S
6A	TB3-11,12	J3L	77	46	6	YES			N
6B	TB5-1,2	J4U	48	26	6	YES			N
7A	TB5-9,10	J6U	42	8	7/9	YES			S
7B	TB5-11,12	J6L	46	18	7/9	YES			S
8A	TB7-1,2	J7U	66	38	8	YES			S
8B	TB7-3,4	J7L	79	48	8	YES			S
PED PUSH BUTTONS									
P21,P22	TB8-4,6	I12U	67	PED 2	2	PED			
P41,P42	TB8-5,6	I12L	69	PED 4	4	PED			
P61,P62	TB8-7,9	I13U	68	PED 6	6	PED			
P81,P82	TB8-8,9	I13L	70	PED 8	8	PED			

NOTE:
 INSTALL DC ISOLATORS IN INPUT FILE SLOTS 112 AND 113.

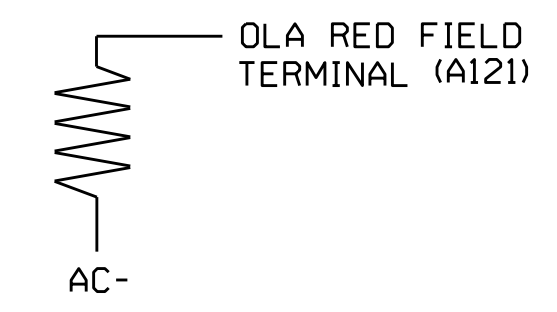
INPUT FILE POSITION LEGEND: J2L



LOAD RESISTOR INSTALLATION DETAIL

(install resistor as shown below)

VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



13-SEP-2016 06:37 S:\IT\SS\115\Sig\ed\work\hgr\oups\g\m\h\mstr\trng\60527_sml.ele.xxx.dgn somstr@ng