

LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. From Main Menu press '2' (PHASE CONTROL), then '1' (PHASE CONTROL FUNCTIONS). Scroll to the bottom of the menu and Enable ACT Logic Commands 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 and 12.
2. From Main Menu press '6' (OUTPUTS), then '3' (LOGICAL I/O PROCESSOR).

LOGICAL I/O COMMAND #1 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON
AND RED CLEAR ON PHASE #1 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #50 ON
SET OUTPUT ASSIGNMENT #51 OFF

Press '+'

LOGICAL I/O COMMAND #2 (+/-COMMAND#)
IF ACTIVE PHASE #1 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #52 OFF

Press '+'

LOGICAL I/O COMMAND #3 (+/-COMMAND#)
IF YELLOW ON PHASE #1 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #51 ON

Press '+'

LOGICAL I/O COMMAND #4 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON
AND RED CLEAR ON PHASE #3 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #47 ON
SET OUTPUT ASSIGNMENT #48 OFF

Press '+'

LOGICAL I/O COMMAND #5 (+/-COMMAND#)
IF ACTIVE PHASE #3 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #49 OFF

Press '+'

LOGICAL I/O COMMAND #6 (+/-COMMAND#)
IF YELLOW ON PHASE #3 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #48 ON

Press '+'

LOGICAL I/O COMMAND #7 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON
AND RED CLEAR ON PHASE #5 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #42 ON
SET OUTPUT ASSIGNMENT #43 OFF

Press '+'

LOGICAL I/O COMMAND #8 (+/-COMMAND#)
IF ACTIVE PHASE #5 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #44 OFF

Press '+'

LOGICAL I/O COMMAND #9 (+/-COMMAND#)
IF YELLOW ON PHASE #5 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #43 ON

Press '+'

LOGICAL I/O COMMAND #10 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON
AND RED CLEAR ON PHASE #7 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #39 ON
SET OUTPUT ASSIGNMENT #40 OFF

Press '+'

LOGICAL I/O COMMAND #11 (+/-COMMAND#)
IF ACTIVE PHASE #7 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #41 OFF

Press '+'

LOGICAL I/O COMMAND #12 (+/-COMMAND#)
IF YELLOW ON PHASE #7 IS ON

↓
SCROLL DOWN

THEN:
SET OUTPUT ASSIGNMENT #40 ON

Press '+'

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

NOTE: Logic for Phase 1 RED Clear when transitioning from Phase 1 to Phase 8 (Head 83).

NOTE: Logic for Switching Flashing Yellow Arrow "OFF" during Phase 1 (Head 83).

NOTE: Logic for Yellow Arrow Clearance from Phase 1 (Head 83).

NOTE: Logic for Phase 3 RED Clear when transitioning from Phase 3 to Phase 2 (Head 23).

NOTE: Logic for Switching Flashing Yellow Arrow "OFF" during Phase 3 (Head 23).

NOTE: Logic for Yellow Arrow Clearance from Phase 3 (Head 23).

NOTE: Logic for Phase 5 RED Clear when transitioning from Phase 5 to Phase 4 (Head 43).

NOTE: Logic for Switching Flashing Yellow Arrow "OFF" during Phase 5 (Head 43).

NOTE: Logic for Yellow Arrow Clearance from Phase 5 (Head 43).

NOTE: Logic for Phase 7 RED Clear when transitioning from Phase 7 to Phase 6 (Head 63).

NOTE: Logic for Switching Flashing Yellow Arrow "OFF" during Phase 7 (Head 63).

NOTE: Logic for Yellow Arrow Clearance from Phase 7 (Head 63).

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

From Main Menu press '8' (OVERLAPS), then '1' (VEHICLE OVERLAP SETTINGS).

PAGE 1: VEHICLE OVERLAP 'A' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: X X
VEH OVL NOT VEH: X
VEH OVL NOT PED: X
VEH OVL GRN EXT: X
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...N
GREEN EXTENSION (0=255 SEC)...0.0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0.0

Press '+'

NOTICE GREEN FLASH

PAGE 1: VEHICLE OVERLAP 'B' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH: X
VEH OVL NOT PED: X
VEH OVL GRN EXT: X
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0=255 SEC)...0.0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0.0

Press '+'

NOTICE GREEN FLASH

PAGE 1: VEHICLE OVERLAP 'C' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH: X
VEH OVL NOT PED: X
VEH OVL GRN EXT: X
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...N
GREEN EXTENSION (0=255 SEC)...0.0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0.0

Press '+'

NOTICE GREEN FLASH

PAGE 1: VEHICLE OVERLAP 'D' SETTINGS
PHASE: 12345678910111213141516
VEH OVL PARENTS: XX
VEH OVL NOT VEH: X
VEH OVL NOT PED: X
VEH OVL GRN EXT: X
STARTUP COLOR: - RED - YELLOW - GREEN
FLASH COLORS: - RED - YELLOW X GREEN

SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0=255 SEC)...0.0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0
OUTPUT AS PHASE # (0=NONE, 1-16)...0.0

Press '+'

NOTICE GREEN FLASH

OVERLAP PROGRAMMING COMPLETE

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

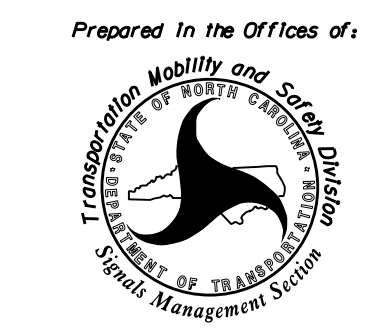
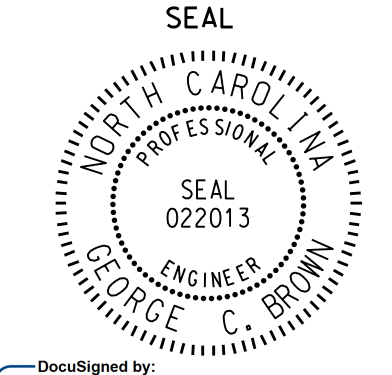
1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-3.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-2.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

OUTPUT REFERENCE SCHEDULE	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 39 =	Overlap D Red
OUTPUT 40 =	Overlap D Yellow
OUTPUT 41 =	Overlap D Green
OUTPUT 42 =	Overlap C Red
OUTPUT 43 =	Overlap C Yellow
OUTPUT 44 =	Overlap C Green
OUTPUT 47 =	Overlap B Red
OUTPUT 48 =	Overlap B Yellow
OUTPUT 49 =	Overlap B Green
OUTPUT 50 =	Overlap A Red
OUTPUT 51 =	Overlap A Yellow
OUTPUT 52 =	Overlap A Green

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 06-1336T3
DESIGNED: June 2015
SEALED: 8/28/15
REVISED: N/A

Electrical Detail - Sheet 2 of 2 - Temp 3 Phase 3

<p>Electrical and Programming Details For:</p> <p>Prepared In the Offices of:</p>  <p>750 N. Greenfield Pkwy, Garner, NC 27529</p>	<p>NC 24-210 (Rowan Street) / NC 24 (Bragg Boulevard) at NC 210 (Murchison Road) / Bragg Boulevard</p> <p>Division 6 Cumberland County Fayetteville</p> <p>PLAN DATE: July 2015 REVIEWED BY:</p> <p>PREPARED BY: B. SIMMONS REVIEWED BY:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>REVISIONS</th> <th>INIT.</th> <th>DATE</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table>	REVISIONS	INIT.	DATE				<p>SEAL</p>  <p>DocuSigned by: <i>George C. Brown</i> 8/31/2015 F12061ED08E8434 DATE</p> <p>SIG. INVENTORY NO. 06-1336T3</p>
REVISIONS	INIT.	DATE						

31-AUG-2015 08:57
 S:\1336T3\SIG\Sig\Work\Programs\Signal\Electrical\Detail\Division 06-1336T3\smc_ele_xxx.dgn
 B.S. SIMMONS