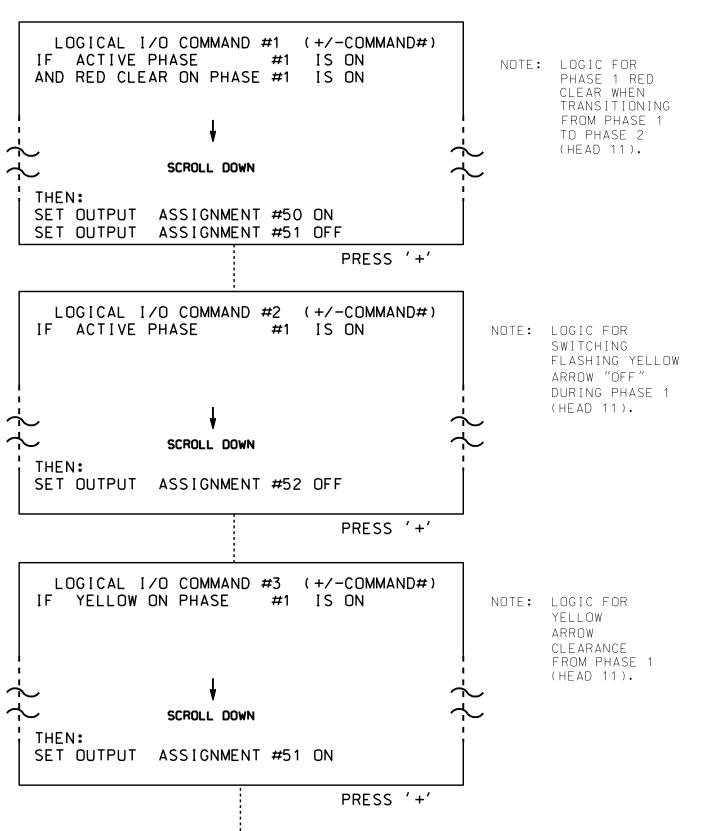
PROJECT REFERENCE NO.

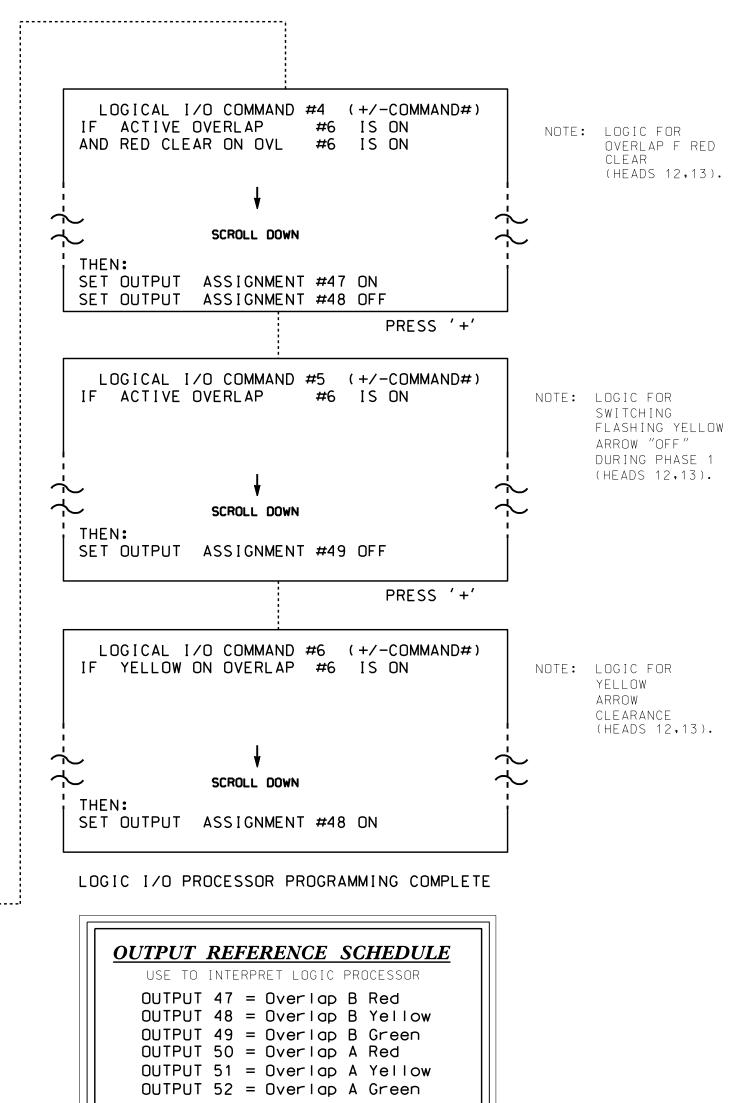
Sig. 3.2

## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5 AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

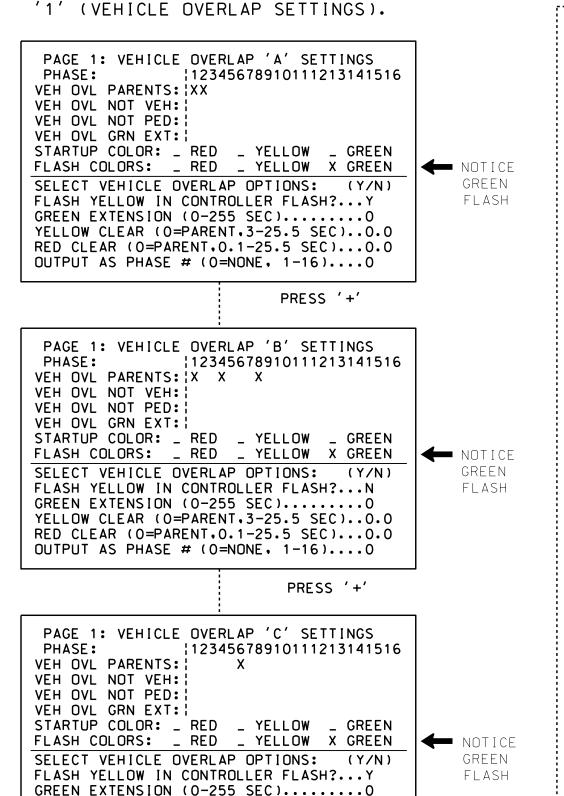




## OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN

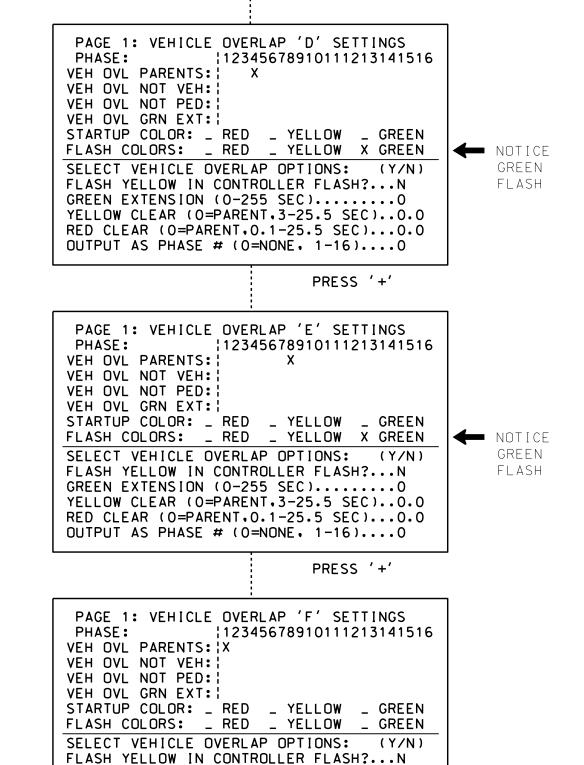


YELLOW CLEAR (O=PARENT.3-25.5 SEC)..0.0

RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0

PRESS '+'

OUTPUT AS PHASE # (0=NONE, 1-16)....0



OVERLAP PROGRAMMING COMPLETE

GREEN EXTENSION (0-255 SEC).....0

OUTPUT AS PHASE # (0=NONE, 1-16)....0

YELLOW CLEAR (O=PARENT,3-25.5 SEC)..0.0

RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0

## FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

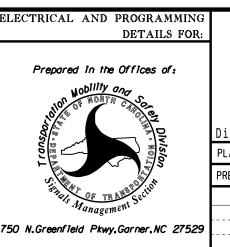
1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.

2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.

3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0871 DESIGNED: October 2015 SEALED: 1/5/2016 REVISED: N/A



Electrical Detail - Sheet 2 of 4 **UNLESS ALL SIGNATURES COMPLETED** US 158 (Clemmons Road) SR 3000 (Idols Road) and

SR 1117 (Old Sides Mill Road)

ivision 9 PLAN DATE: December 2015 REVIEWED BY: PREPARED BY: C. Strickland REVIEWED BY: REVISIONS INIT. DATE

SIG. INVENTORY NO. 09-0871

DOCUMENT NOT CONSIDERED FINAL