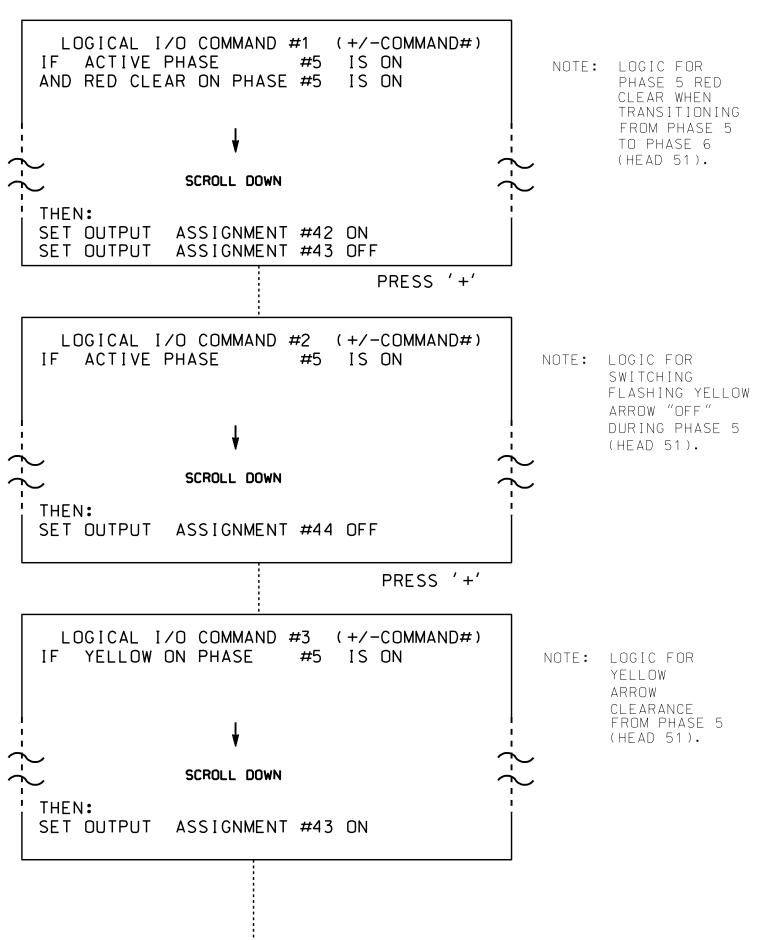
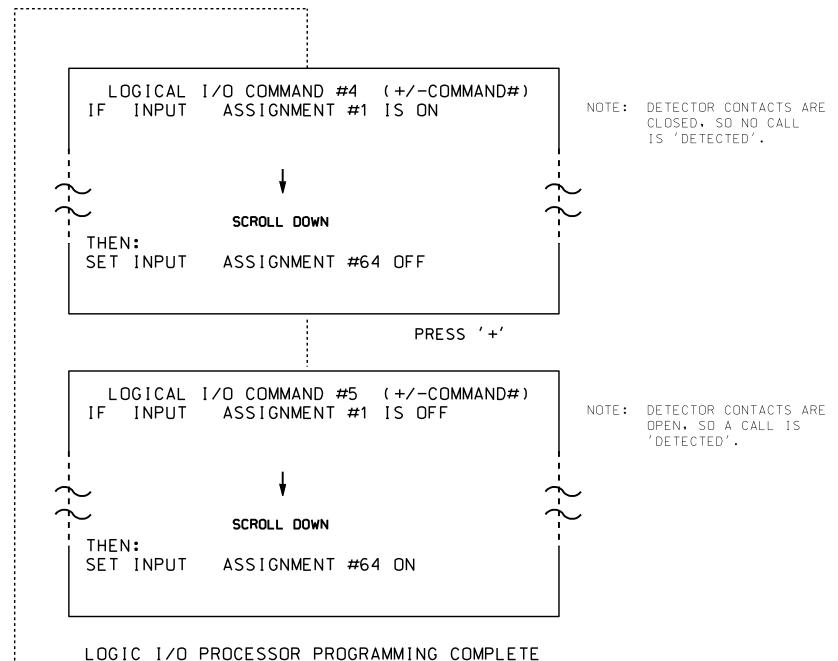
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, AND 5.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).





OUTPUT REFERENCE SCHEDULE

INPUT 1 = Detector Physical Input (Not Enabled) INPUT 64 = Dummy Detector Input (Detector 2) OUTPUT 42 = Overlap C Red OUTPUT 43 = Overlap C Yellow

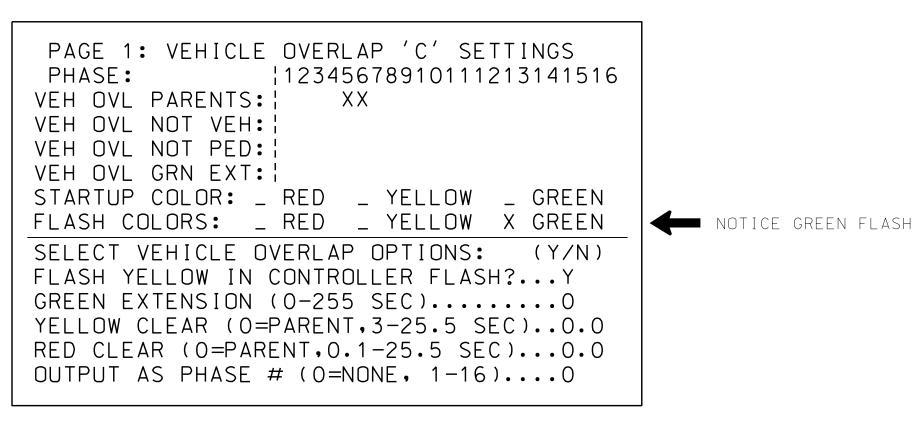
OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).

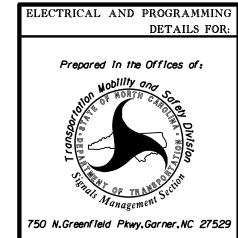
PRESS '+' TWICE



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1592 DESIGNED: March 2014 SEALED: 4/1/2015 REVISED: N/A

Electrical Detail - Sheet 2 of 3



SR 1486 (Greensboro Road)

I-74 WB/US 311 NB Ramps

Guilford County ____ps High Point ivision 7 PLAN DATE: May 2014 REVIEWED BY: 978

PREPARED BY: S. Armstrong | REVIEWED BY:

SEAL

008453

REVISIONS INIT. DATE SIG. INVENTORY NO. 07-1592