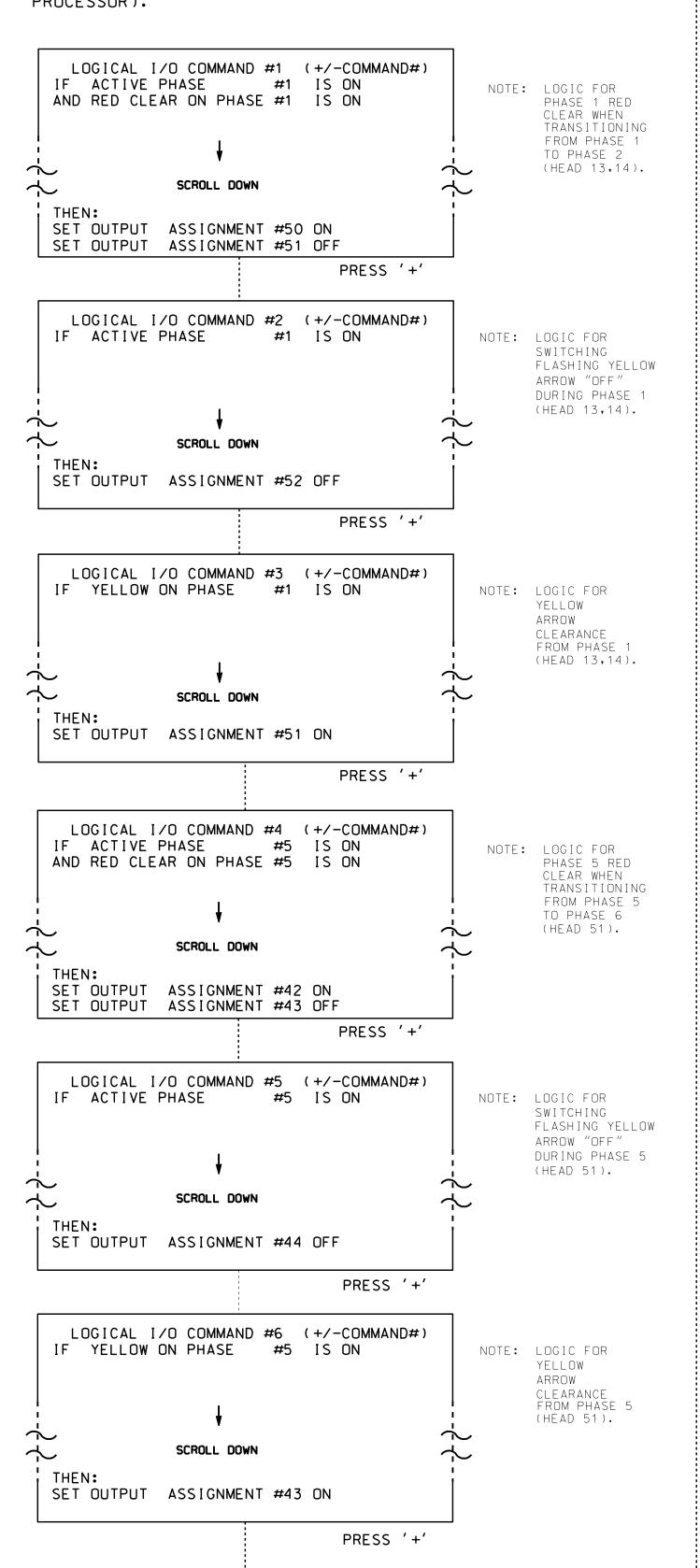
## Sig.124.

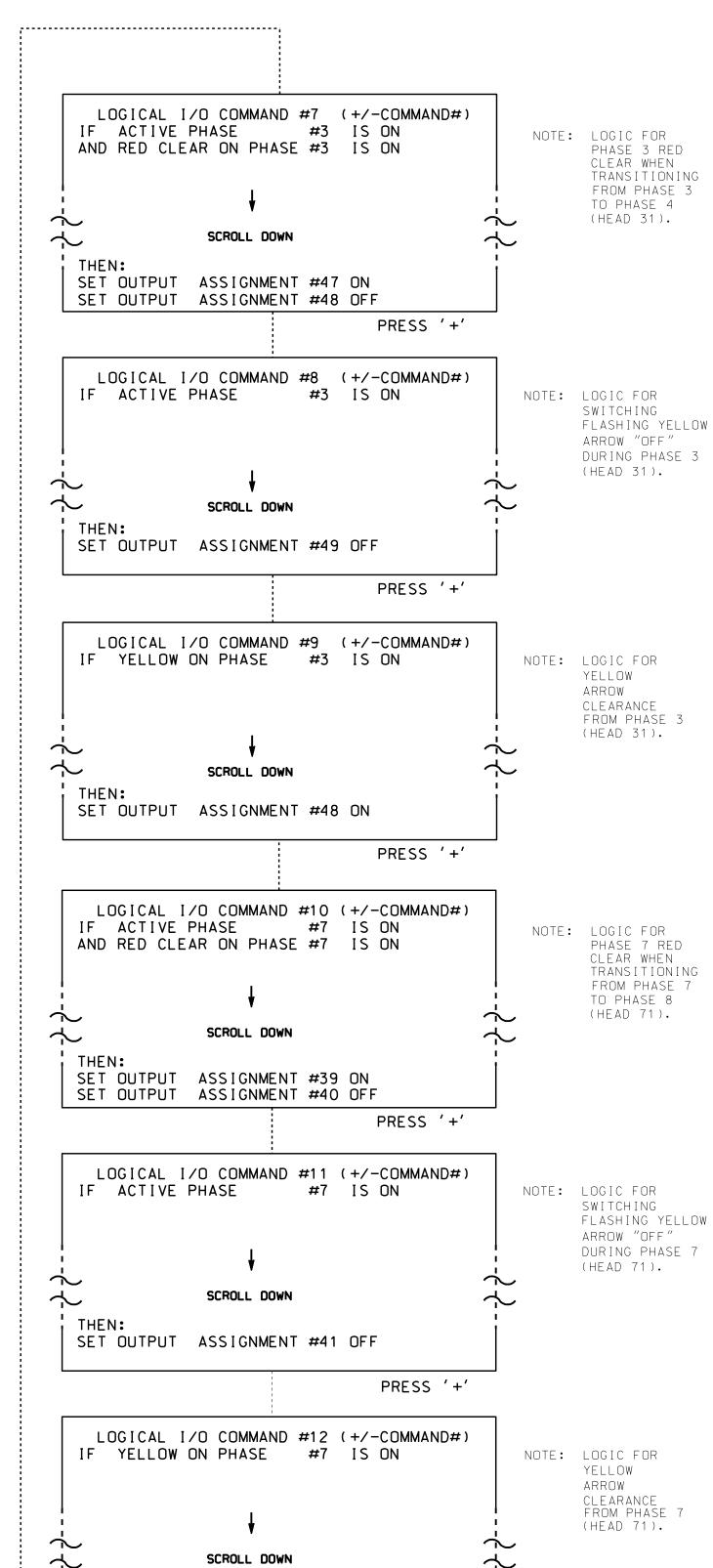
## LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, AND 12.

2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



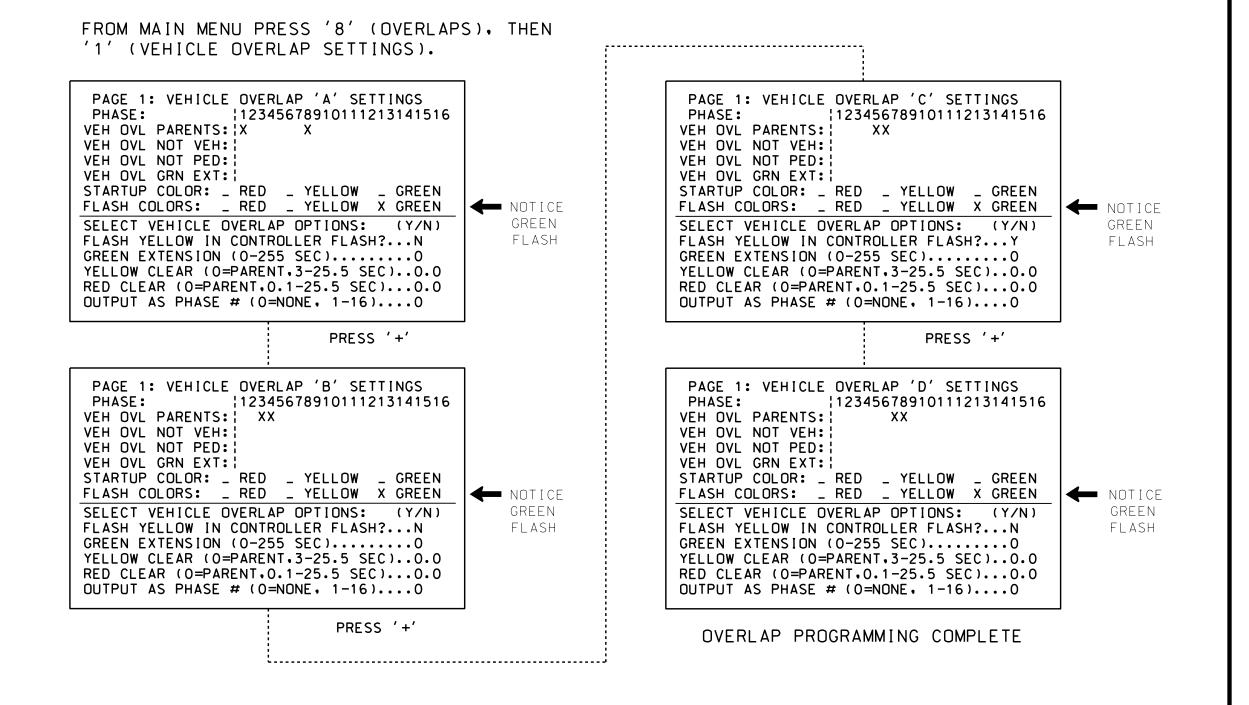


SET OUTPUT ASSIGNMENT #40 ON

LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

## OVERLAP PROGRAMMING <u>DETAIL</u>

(program controller as shown below)

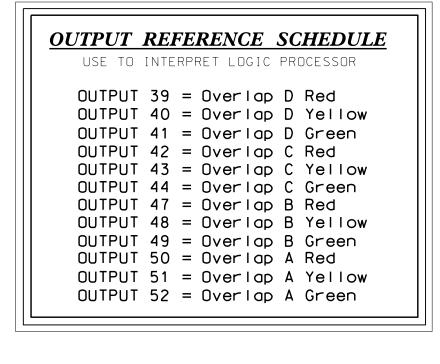


## FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

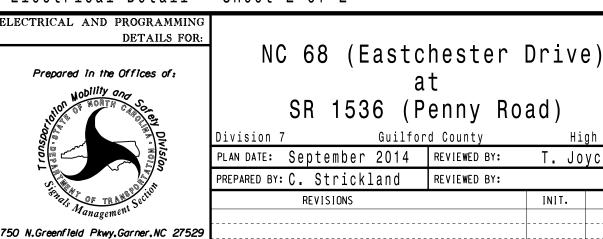
- 1. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- 2. ON REAR OF PDA REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- 3. REMOVE FLASHER UNIT 2.

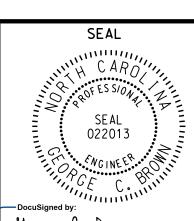
THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.



THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-1527 DESIGNED: September 2014 SEALED: 4/22/2015 REVISED: N/A

Electrical Detail - Sheet 2 of 2





High Point

T. Joyce

INIT. DATE

George C. Brown 4/29/2015 SIG. INVENTORY NO. 07-1527