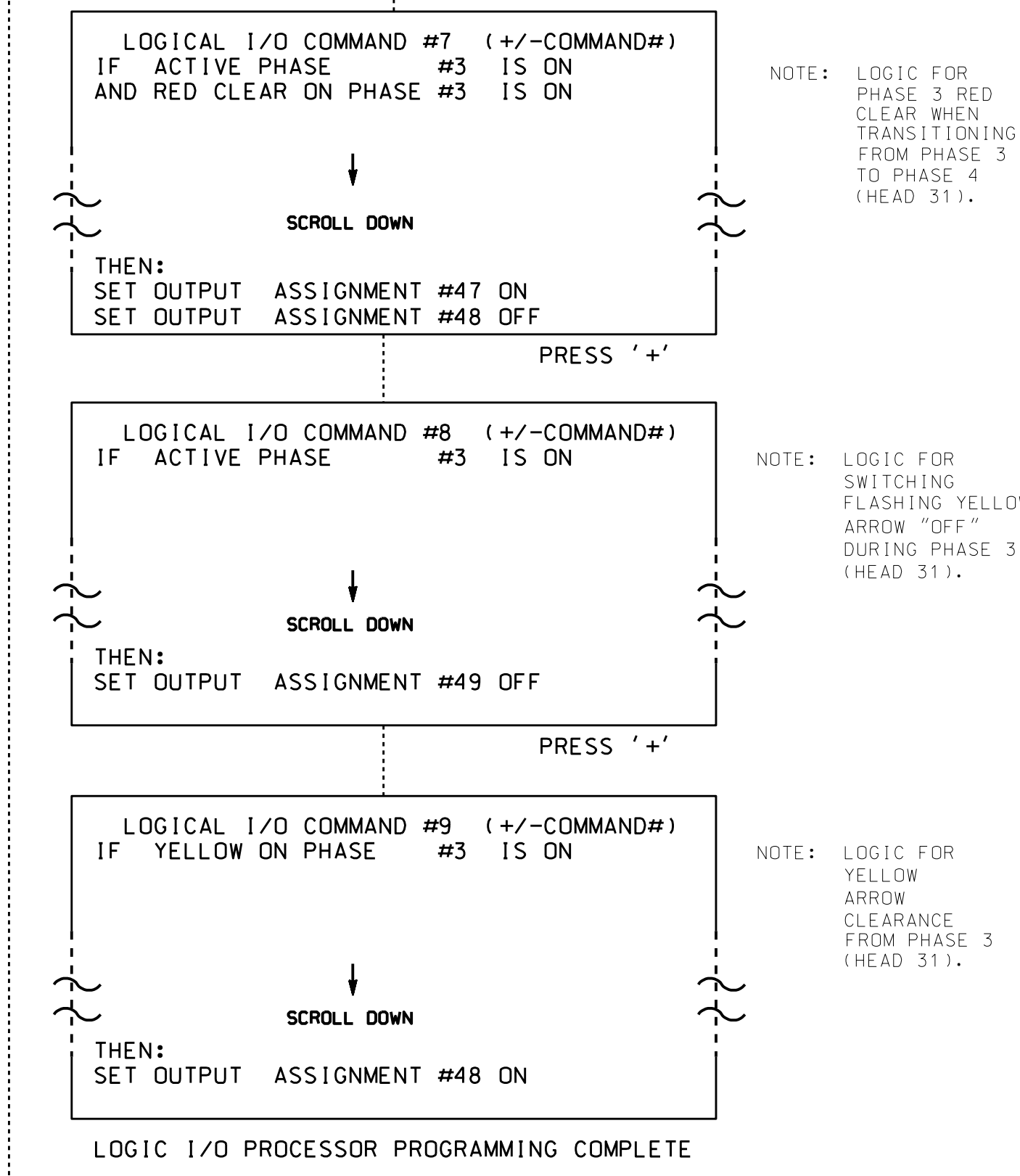
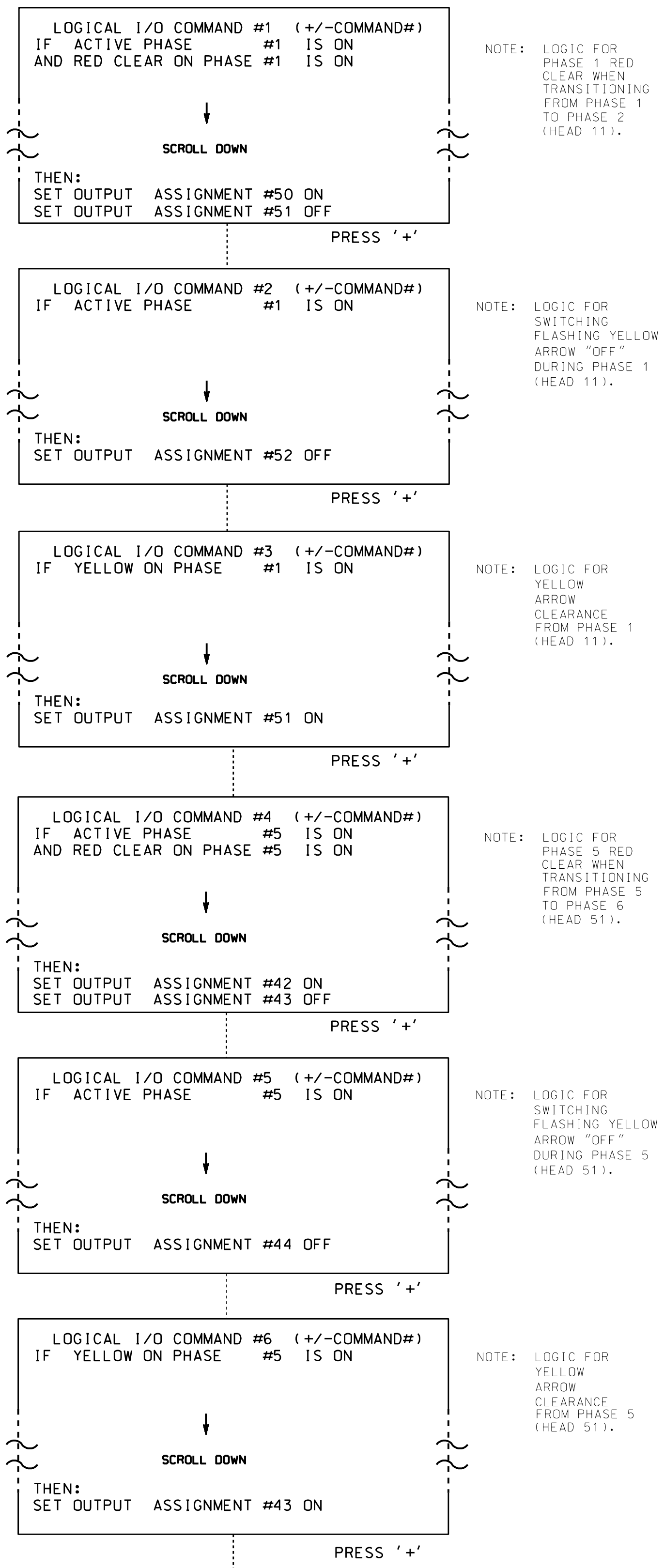


LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS), SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, 3, 4, 5, 6, 7, 8 and 9.
2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).

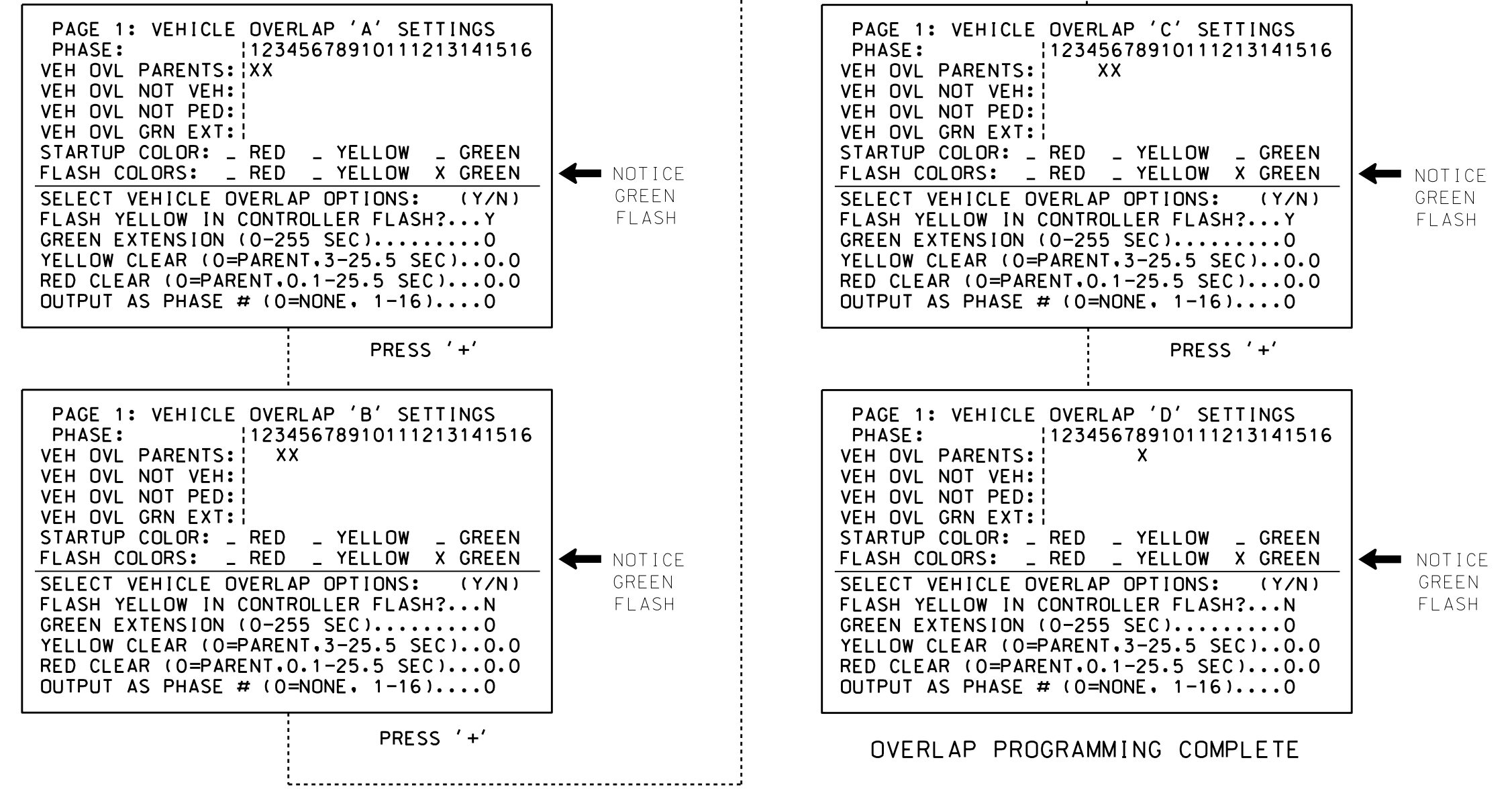


LOGIC I/O PROCESSOR PROGRAMMING COMPLETE

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

1. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
2. ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
3. REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

OUTPUT REFERENCE SCHEDULE	
USE TO INTERPRET LOGIC PROCESSOR	
OUTPUT 42 =	Overlap C Red
OUTPUT 43 =	Overlap C Yellow
OUTPUT 44 =	Overlap C Green
OUTPUT 47 =	Overlap B Red
OUTPUT 48 =	Overlap B Yellow
OUTPUT 49 =	Overlap B Green
OUTPUT 50 =	Overlap A Red
OUTPUT 51 =	Overlap A Yellow
OUTPUT 52 =	Overlap A Green

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 07-0947
DESIGNED: October 2014
SEALED: 3-30-15
REVISED: N/A

ELECTRICAL DETAIL SHEET 2 OF 2

	Prepared in the Offices of: SR 1961 (W. Market Center Dr.) SR 1962 (S. College Dr.) at SR 4053 (Surrett Dr.)	SEAL
ELECTRICAL AND PROGRAMMING DETAILS FOR:	Division 7 Guilford County High Point	PLAN DATE: October 2014 REVIEWED BY: JTR
PREPARED BY: James Peterson	REVIEWED BY:	REVISIONS INIT. DATE
DocuSigned by: John T. Rowe, Jr. 4/7/2015		SIG. INVENTORY NO. 07-0947

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 J.peterson