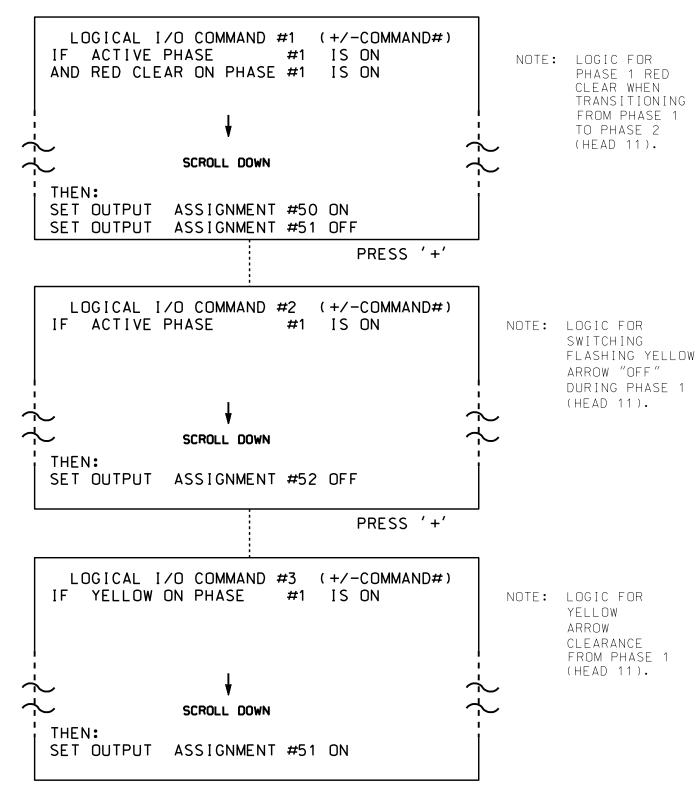
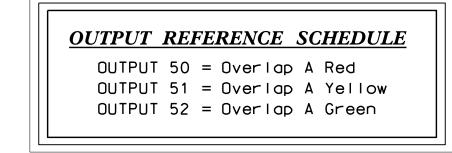
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3. IF ENABLED, DISABLE ACT LOGIC COMMANDS 4, 5 AND 6.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



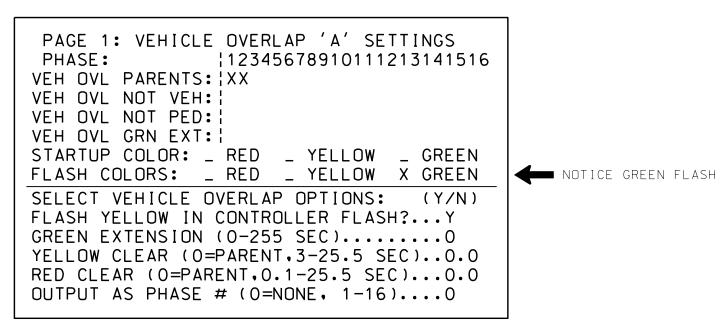
LOGIC I/O PROCESSOR PROGRAMMING COMPLETE



OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

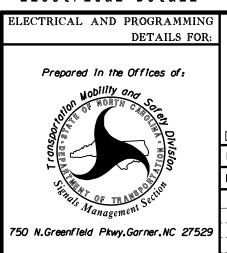
FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).



OVERLAP PROGRAMMING COMPLETE

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 09-0735T2 DESIGNED: May 2015 SEALED: 07/01/2015 REVISED: N/A

Electrical Detail - Temp 2 - Sheet 2 of 2



	NC 8	(W	insto	n Road	<u>(</u>		
			at				
)	Bus./US	29	SB-US	64-70	WB	Ramp	

Division 9	Davidso	n County	Lexington
PLAN DATE:	June 2015	REVIEWED BY:	
PREPARED BY: C	Strickland	REVIEWED BY:	

C. Strickland REVIEWED BY:

REVISIONS INIT. DATE

CBB9728901A2497... DATE

SIG. INVENTORY NO. 09 - 0735T2

SEAL

09-JUL-2015 14:36 S:*ITS&SU*ITS Signals*Workgroups*Sig Man*Strickland*090735 cestrickland