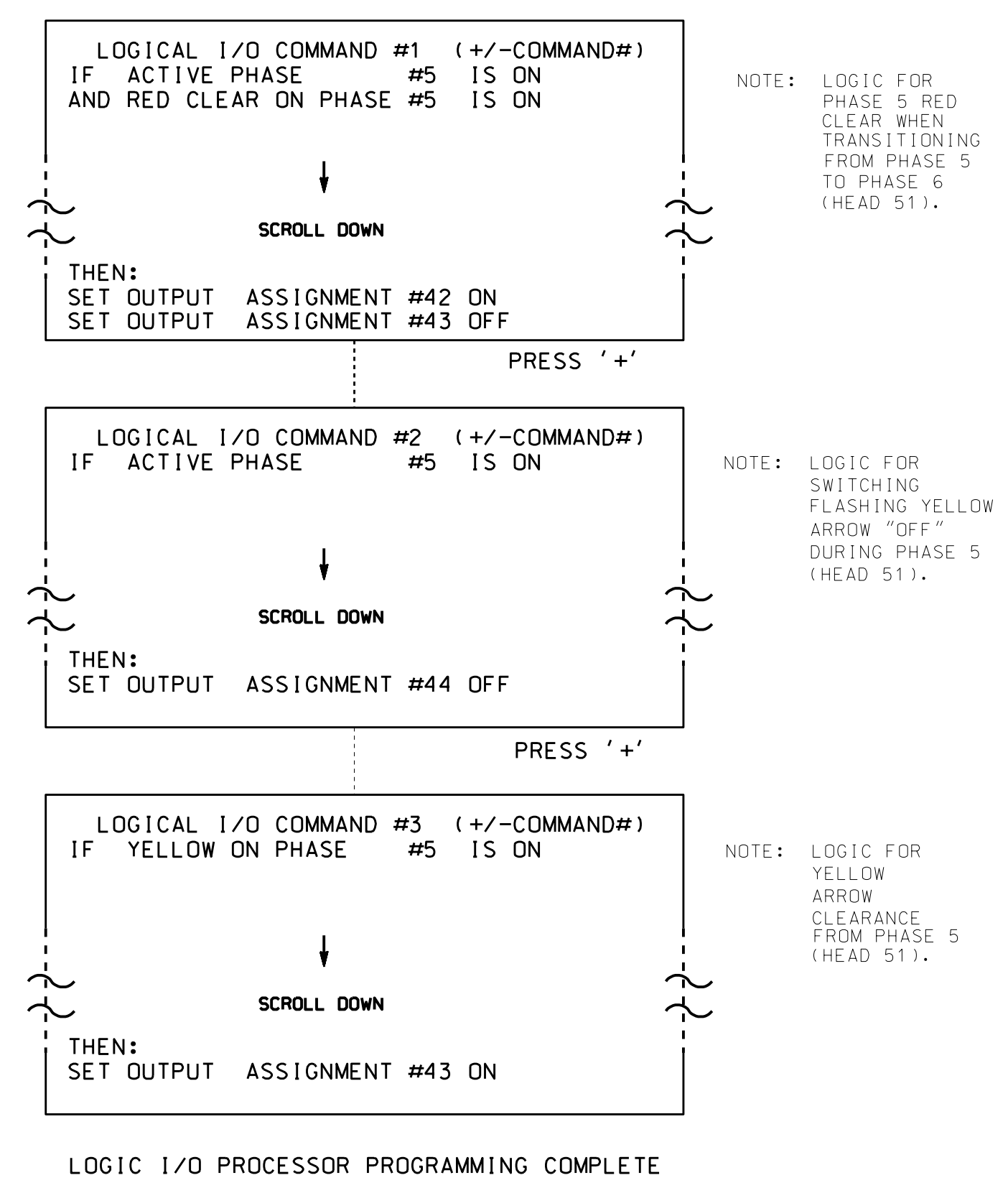


**LOGICAL I/O PROCESSOR PROGRAMMING DETAIL
TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE**

(program controller as shown below)

- FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2 AND 3.
- FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



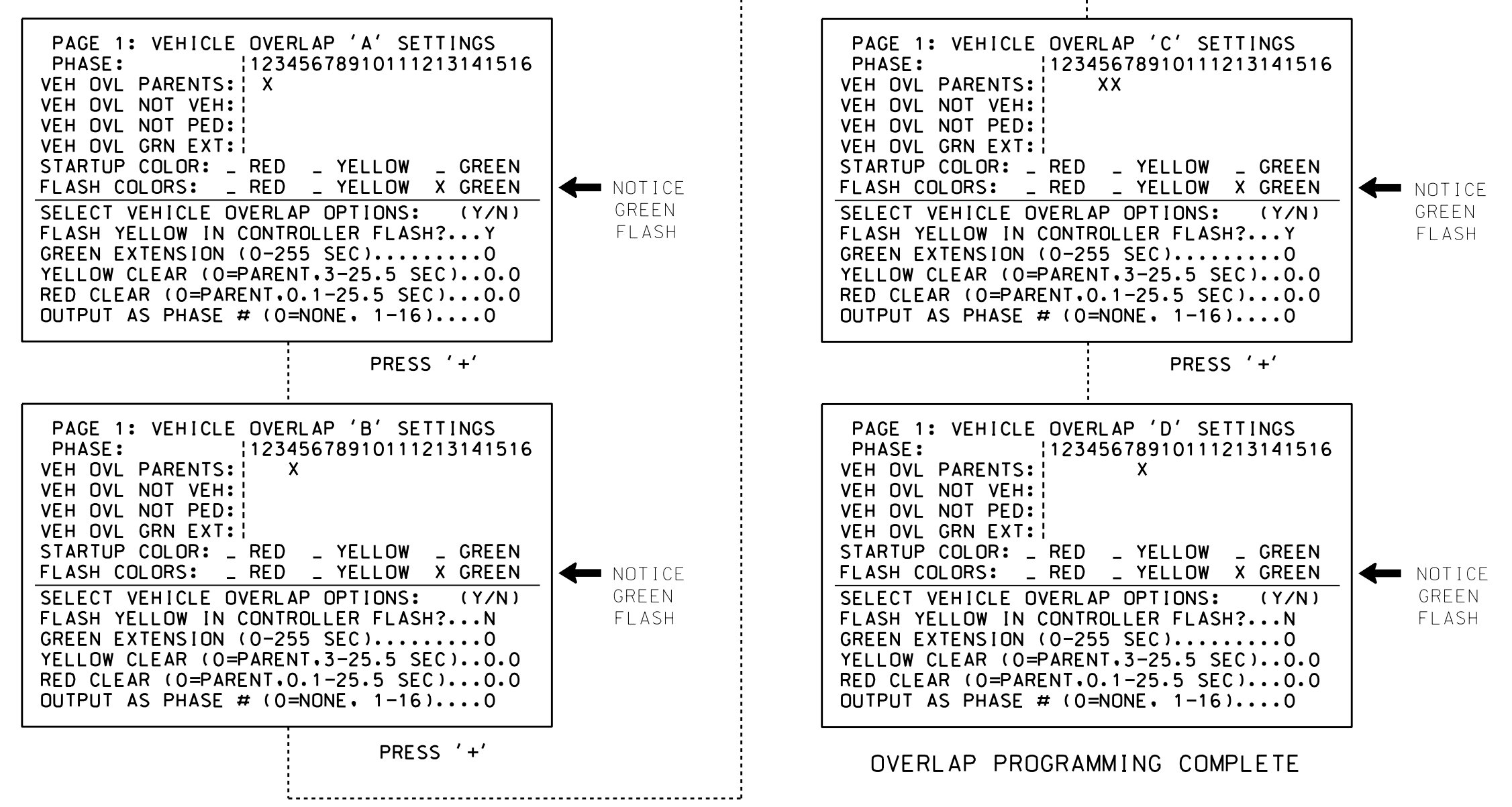
OUTPUT REFERENCE SCHEDULE

OUTPUT 42 = Overlap C Red
OUTPUT 43 = Overlap C Yellow
OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL

(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS), THEN '1' (VEHICLE OVERLAP SETTINGS).



FLASHER CIRCUIT MODIFICATION DETAIL

IN ORDER TO INSURE THAT SIGNALS FLASH CONCURRENTLY ON THE SAME APPROACH, MAKE THE FOLLOWING FLASHER CIRCUIT CHANGES:

- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-4 AND TERMINATE ON T2-2.
- ON REAR OF PDA - REMOVE WIRE FROM TERM. T2-5 AND TERMINATE ON T2-3.
- REMOVE FLASHER UNIT 2.

THE CHANGES LISTED ABOVE TIES ALL PHASES AND OVERLAPS TO FLASHER UNIT 1.

THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 08-0506
DESIGNED: March 2014
SEALED: 4-01-15
REVISED: N/A

ELECTRICAL DETAIL SHEET 2 OF 2

<p>Prepared in the Offices of:</p>	<p>NC 49 at SR 1144 (Mack Road)</p>		<p>SEAL JOHN T. ROWE, JR. ENGINEER SEAL 008453</p>
	<p>Division 8 Randolph County, NC Asheville</p> <p>PLAN DATE: April 2014 REVIEWED BY: JTR</p> <p>PREPARED BY: James Peterson REVIEWED BY:</p>	<p>DocuSigned by: John T. Rowe, Jr. 4/8/2015</p> <p>SIG. INVENTORY NO. 08-0506</p>	

07-08-2015 13:34
 S:\IT\25314\T5\Sigma\work\kg\080506_sml.ele_20140415.dgn
 J.peterson