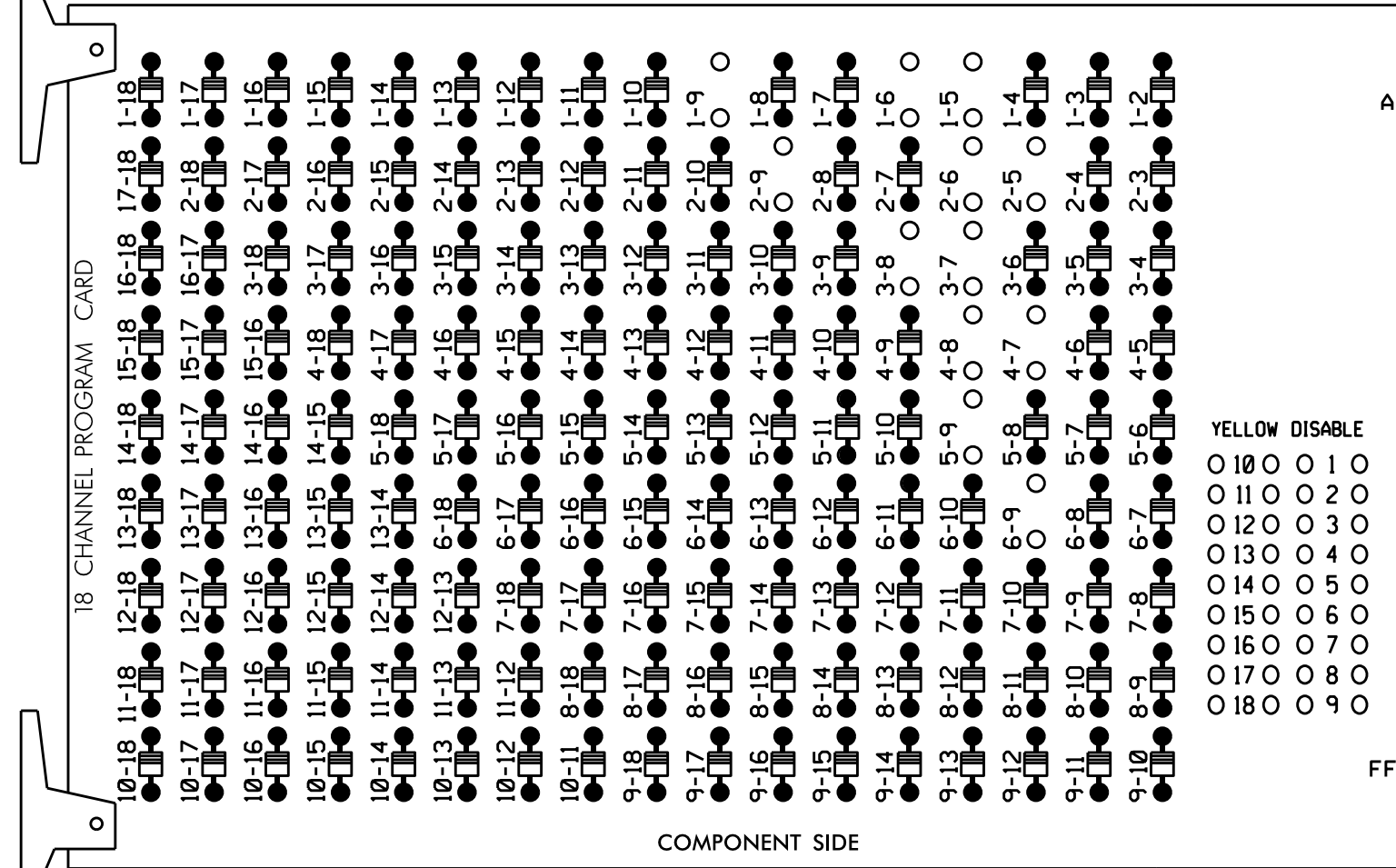


**EDI MODEL 2018ECL-NC CONFLICT MONITOR**

**PROGRAMMING DETAIL**

(remove jumpers and set switches as shown)

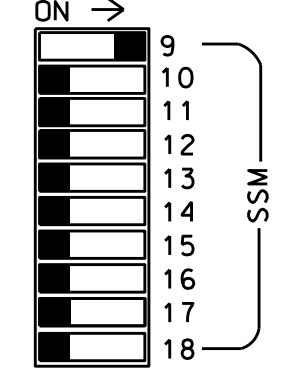
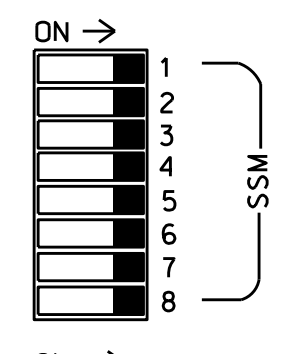
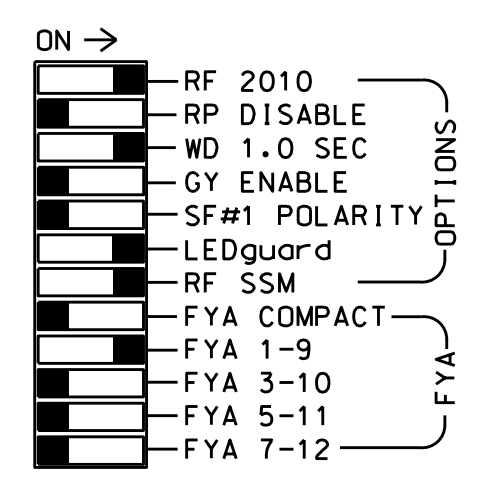
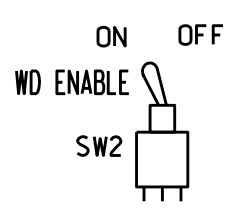
REMOVE DIODE JUMPERS 1-5, 1-6, 1-9, 2-5, 2-6, 2-9, 3-7, 3-8, 4-7, 4-8, 5-9, and 6-9.



REMOVE JUMPERS AS SHOWN

**NOTES:**

1. Card is provided with all diode jumpers in place. Removal of any jumper allows its channels to run concurrently.
2. Ensure jumpers SEL2-SEL5 and SEL9 are present on the monitor board.
3. Ensure that Red Enable is active at all times during normal operation.
4. Connect serial cable from conflict monitor to comm. port 1 of 2070 controller. Ensure conflict monitor communicates with 2070.



■ = DENOTES POSITION OF SWITCH

**SIGNAL HEAD HOOK-UP CHART**

LOAD SWITCH NO.	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	AUX S1	AUX S2	AUX S3	AUX S4	AUX S5	AUX S6				
CMU CHANNEL NO.	1	2	13	3	4	14	5	6	15	7	8	16	9	10	17	11	12	18				
PHASE	1	2	2 PED	3	4	4 PED	5	6	6 PED	7	8	8 PED	OLA	OLB	SPARE	OLC	OLD	SPARE				
SIGNAL HEAD NO.	11	82	21,22	NU	22	31	41,42	NU	42	51,52	61,62	NU	62	71,72	81,82	NU	11	NU	NU	NU	NU	
RED		*	128			101				134			107									
YELLOW			129			102				135			108									
GREEN			130			103				136			109									
RED ARROW					116			131			122		A121									
YELLOW ARROW		126		117	117			132	132		123	123		A122								
FLASHING YELLOW ARROW														A123								
GREEN ARROW	127	127		118	118			133	133		124	124										

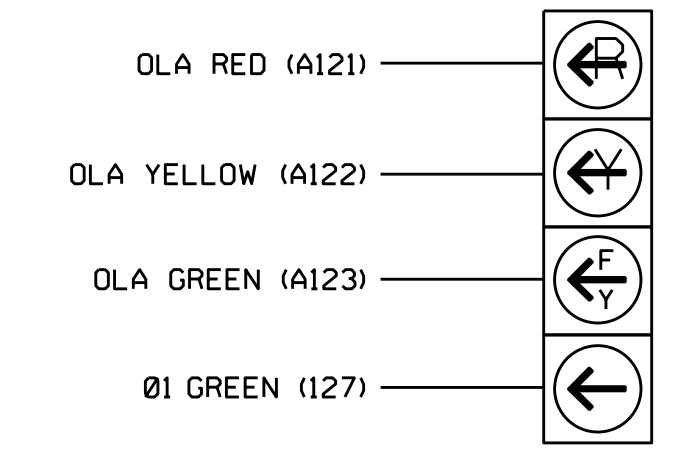
NU = Not Used

\* Denotes install load resistor. See load resistor installation detail this sheet.

★ See pictorial of head wiring this sheet.

**FYA SIGNAL WIRING DETAIL**

(wire signal head as shown)



11

**NOTE**

The sequence display for signal head 11 requires special logic programming. See sheet 2 for programming instructions.

**NOTES**

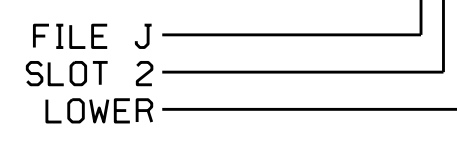
1. To prevent "flash-conflict" problems, insert red flash program blocks for all unused vehicle load switches in the output file. The installer shall verify that signal heads flash in accordance with the Signal Plans.
2. Enable Simultaneous Gap-Out for all phases.
3. Program phases 2 and 6 for Variable Initial and Gap Reduction.
4. Program phases 2 and 6 for Start Up In Green.
5. Program phases 2 and 6 for Yellow Flash, and overlap 1 as Wag Overlaps.

**INPUT FILE CONNECTION & PROGRAMMING CHART**

LOOP NO.	LOOP TERMINAL	INPUT FILE POS.	PIN NO.	INPUT ASSIGNMENT NO.	DETECTOR NO.	NEMA PHASE	CALL	EXTEND	FULL TIME DELAY	STRETCH TIME	DELAY TIME
1A <sup>1</sup>	TB2-1,2	I1U	56	18	1	1	Y	Y			15
1B	TB2-5,6	I2U	39	1	2	1	Y	Y	Y		3
2A	TB2-9,10	I3U	63	25	32	2	Y	Y			15
2B	TB2-11,12	I3L	76	38	42	2	Y	Y			
3A	TB4-5,6	I5U	58	20	3	3	Y	Y			
4A	TB4-9,10	I6U	41	3	4	4	Y	Y			
4B	TB4-11,12	I6L	45	7	14	4	Y	Y			
5A	TB3-1,2	J1U	55	17	5	5	Y	Y			
5B	TB3-3,4	J1L	55	17	5	5	Y	Y			
5C	TB3-5,6	J2U	40	2	5	5	Y	Y			15
6A	TB3-9,10	J3U	64	26	36	6	Y	Y			
6B	TB3-11,12	J3L	77	39	46	6	Y	Y			
7A	TB5-5,6	J5U	57	19	7	7	Y	Y			
7B	TB5-7,8	J5L	57	19	7	7	Y	Y			
8A	TB5-9,10	J6U	42	4	8	8		Y		2,4	
8B	TB5-11,12	J6L	46	8	18	8		Y		2,4	
8C	TB7-1,2	J7U	66	28	38	8	Y	Y			
8D	TB7-3,4	J7L	79	41	48	8	Y	Y			

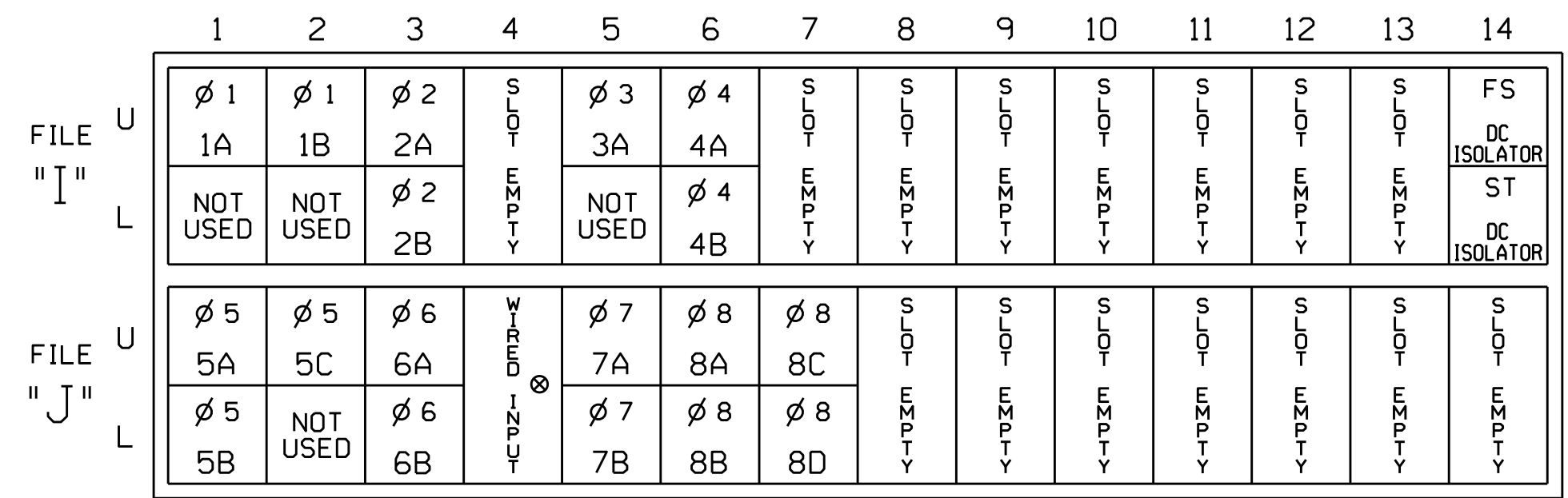
<sup>1</sup>Add jumper from I1-W to J4-W, on rear of input file.

**INPUT FILE POSITION LEGEND: J2L**



**INPUT FILE POSITION LAYOUT**

(front view)



EX.: 1A, 2A, ETC. = LOOP NO.'S

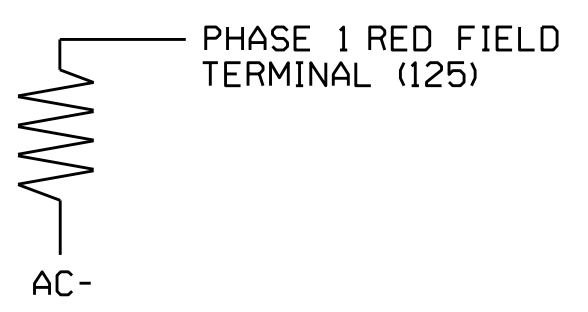
FS = FLASH SENSE  
ST = STOP TIME

⊗ Wired Input - Do not populate slot with detector card

**LOAD RESISTOR INSTALLATION DETAIL**

(install resistor as shown below)

ACCEPTABLE VALUES	
VALUE (ohms)	WATTAGE
1.5K - 1.9K	25W (min)
2.0K - 3.0K	10W (min)



THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 11-0341  
DESIGNED: September 2014  
SEALED: 10/14/2014  
REVISED: N/A

Electrical Detail - Final Design - Sheet 1 of 2

ELECTRICAL AND PROGRAMMING DETAILS FOR: Prepared In the Offices of: 750 N. Greenfield Pkwy, Garner, NC 27529	US 221-NC 194 at US 221 Business-NC 194/NC 163	SEAL 
	Division 11 PLAN DATE: October 2014 PREPARED BY: S. Armstrong	Ashe County REVIEWED BY: JTR REVIEWED BY: