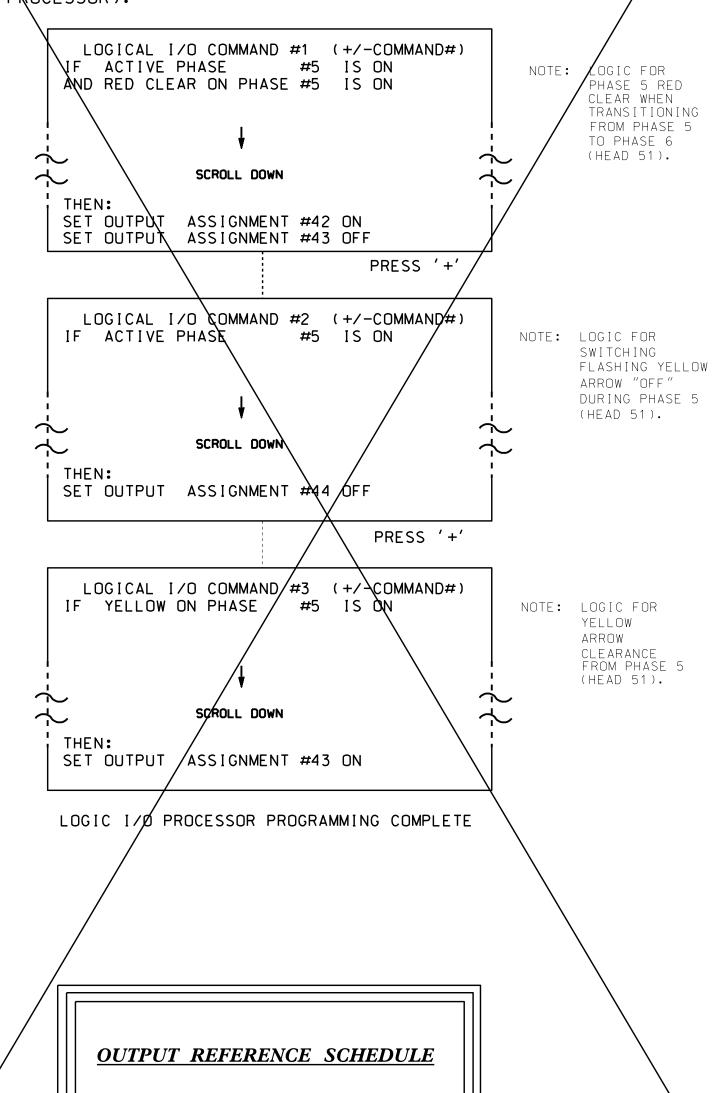
LOGICAL I/O PROCESSOR PROGRAMMING DETAIL TO PRODUCE SPECIAL FYA-PPLT SIGNAL SEQUENCE

(program controller as shown below)

- 1. FROM MAIN MENU PRESS '2' (PHASE CONTROL), THEN '1' (PHASE CONTROL FUNCTIONS). SCROLL TO THE BOTTOM OF THE MENU AND ENABLE ACT LOGIC COMMANDS 1, 2, AND 3.
- 2. FROM MAIN MENU PRESS '6' (OUTPUTS), THEN '3' (LOGICAL I/O PROCESSOR).



OUTPUT 42 = Overlap C Red

OUTPUT 43 = Overlap C Yellow

OUTPUT 44 = Overlap C Green

OVERLAP PROGRAMMING DETAIL

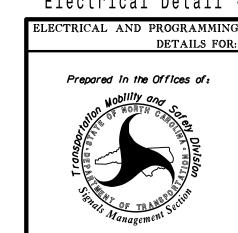
(program controller as shown below)

FROM MAIN MENU PRESS '8' (OVERLAPS). THEN '1' (VEHICLE OVERLAP SETTINGS).

PRESS '+' TWLE PAGE 1: VEHICLE OVERLAP 'C' SETTINGS \1234567891011121*3*141516 PHASE: VEH OVL PARENTS: XX VEH OVL NOT VEH: VEH OVL GRN EXT STARTUP COLOR: _ RED _ YELLOW _ GREEN FLASH COLORS: _ RED _ YELLOW X GREEN NOTICE GREEN FLASH SELECT VEHICLE OVERLAP OPTIONS: (Y/N)
FLASH YELLOW IN CONTROLLER FLASH?...Y
GREEN EXTENSION (0-255 SEC)......0
YELLOW CLEAR (0=PARENT.3-25.5 SEC)...0.0
RED CLEAR (0=PARENT.0.1-25.5 SEC)...0.0 OUTPUT AS PHASE # (0=NONE, 1-16)...0 OVERLAP PROGRAMMING COMPLETE

> THIS ELECTRICAL DETAIL IS FOR THE SIGNAL DESIGN: 11-0341T4 DESIGNED: September 2014 SEALED: 10/14/2014 REVISED: N/A

Electrical Detail - Temporary Design 4 - TCP Phase III (Step 5) - Sheet 2 of 2



US 221-NC 194 US 221 Business-NC 194/NC 163

Division	4.4	A - b -	0	W	10 f f o no o n
Division	11	ASTIE	County	nea _{bs} west	Jefferson
PLAN DATE:	October	2014	REVIEWED BY:	STR	

PREPARED BY: S. Armstrong Reviewed BY: INIT. DATE SIG. INVENTORY NO. 11-0341T4